Journal of Advanced Research in Technology and Management Sciences
Volume: 01 Issue: 03 ISSN: 2582-307 November 2019
Available online at: http://www.jartms.org

A NOVEL DESIGN AND IMPLEMENTATION OF 7T SRAM ARRAY WITH 28 NM TECHNOLOGY USING SVL METHOD

[1]SHAIK NANNU SAHEB, [2]Dr .RAMESH MARPU, [3]Dr.PRABODH KHAMPARIYA
[1]Research Scholar, Sri Satya Sai University of Technology & Medical Sciences, Sehore, Madhya Pradesh, India.
[2]Professor, Vaageswari College of Engineering, Karimnagar, Telangana, India.
[3]Reserach Guide, Sri Satya Sai University of Technology & Medical Sciences, Sehore, Madhya Pradesh, India.

ABSTRACT: Static Random Access Memory (SRAM) has become a major component in many VLSI Chips due to their large storage density and small access time. SRAM has become the topic of substantial research due to the rapid development for low power memory design during recent years due to increase demand for notebooks, laptops, IC memory cards and hand held communication devices. SRAMs are widely used for mobile applications as both on chip and off-chip memories, because of their ease of use and low power consumption. In the performance of memory cell, delay and power consumption plays a major role. Random-Access Memory employs latching circuitry to store data and preserve the bits MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) help compensate for the SRAM cells. In addition, improvements withinside the System of Chip are essential. In this work, a novel design and implementation of 7T SRAM array with 28 nm technology using SVL (self-controllable Voltage Level) method is presented. The main objective of this work is to reduce the leakage power of SRAM array. The SVL method is used to analyze the consumption of power, leakage power and current parameters of 7T (7- Transistor) SRAM array.

KEYWORDS: Static Random Access Memory (SRAM), MOSFET, 7T SRAM, power reduction.

I. INTRODUCTION

Static random access memory power and speed dissipation are the significant factor in most of the electronic applications, which prompts numerous plans with the power utilization of limiting the power during the hold, write, and read processes. One of the important parts of CMOS IC (complementary metal oxide semiconductor integrated circuit) is the memory.

Static random-access memory is a type of semiconductor memory that uses bi-stable latching circuitry to store each bit. The term static differentiates it from dynamic RAM which must be periodically refreshed. SRAM exhibits data remembrance, but is still volatile in conventional sense, that data is eventually lost when memory is not powered. SRAM cell is a high-speed memory cell that is used for high-speed applications like buffers and caches.

The reason SRAM is used in this application is that it is faster than DRAM which is also used as a memory cell but it is constituted of capacitors while the other hand SRAM is constituted of transistors. The growing market of portable battery-operated systems demands micro-electronic circuit design with ultra low power dissipation. This emerging portable SoC designs demand for low power SRAMs. The SRAM is one of the integral segments of SoC (System-on-Chip) design.

In portable electronic devices, the SoCs have certain requirements such as high speed and less power operation modes. In low power operation modes, the SRAM in a SoC might be operated at lower voltages whereas in high speed operation it operates at high voltages. The SRAM is one of the integral segments of SoC (Syste-on-Chip) design. The embedded chips include essential elements which make a major contribution to overall power / energy use in the static random access memory devices. Nonetheless, owing to the severe damage in the noise margin with static read and the capacity with write enable, in

addition to the rigorous impacts of the leakage current with read bit line, a regular six transistor (6T). SRAM track usually supplied by the foundry has not been ranged to near/ sub-threshold values. The most normally utilized 6T SRAM cell has the detriment of keeping up essential Read Noise Margin (RNM) and Write Noise Margin (WNM) as the innovation is downsized. To conquer this, SRAM cells with 7T, 8T and 9T are built to cast and accomplish preferable outcomes over the regular 6T cell.

In the current mobile market, large number of electronic systems and applications depend on semiconductor solid state memories. The performance needed by new electronic devices pushes towards ultra-low power storage media. Designing an ultralow power Static Random Access Memory circuit is vital for embedded chips used in wearable or portable electronics components. The topology of the Static Random Access Memory cell is revamped to allow many numbers of transistors to maximize the noise gap with static read, also to boost write performance, and decrease the leakage present in read bitline.

The overall power optimization of the system would largely depend on the performance of static random-access memory (SRAM) due to its wide-scale use as microprocessor caches. Supply voltage scaling has been the most attractive approach until recently to reduce the overall power consumption. However, this leads to a significant increase in delay. Moreover, increased leakage current and reduced ON-current are serious drawbacks at lower *V*dd. Power utilization is also considered as of the main factors along with speed and cost. To overcome this, we employ an SVL (self-voltage level) circuit in connection with SRAM cells. Self-controllable voltage level is a technique in which PMOS (P-channel Metal Oxide Semiconductor) transistor acts as a switch and NMOS (N-channel Metal Oxide Semiconductor) transistors act as a resistors coupled in series reduces leakage current when the transistors change its state from sleep to active and vice versa. Hence, in this work a novel design and implementation of 7T SRAM array with 28 nm technology using SVL method.

The rest of the paper is organized as follows: The section II describes the related work. The section III demonstrates presented 7T SRAM array with 28 nm technology using SVL method. The section IV describes the result analysis and finally this work is concluded in section V.

II. LITERATURE SURVEY

Beram Eswar Charan Teja, M. Damodhar Rao, Dr. Y. V. Narayana and Dr. V. V. K. D. V. Prasad et. al., [1] presents Design & Implementation of Improved SRAM Cell. The main objective of this project is to design low power consumption SRAM cell and SRAM array for embedded applications. The conventional 6T SRAM cell is implemented in 180, 65 and 45nm technologies and compared with 7T, 8T and 9T SRAM cells in terms of power. By the comparison of conventional 6T SRAM Cell and 4X4 array with 7T, 8T and 9T SRAM cells with the help of HSpice tool, the 8T SRAM single cell and 4X4 array with transmission gate consumes low power.

Pulla Reddy A, G Sreenivasulu, R Veerabadra Chary et. al., [2] presents Write and Read Assist Techniques for SRAM Memories in Nanometer Technology. In this paper various write and read assist techniques are analyzed with their pros and cons and each technique is explained with their implementation and their impact on write-ability, readability and stability of the SRAM memory. The SRAM bit cell write-ability is very critical at lower voltages. The impacts of the write assist technique

analyzed across the process, voltage and temperature range. Along with improving the write-ability of the SRAM cell the write assist techniques will impact the performance, power and area of the chip.

Apoorva Pathak, Divyesh Sachan, Harish Peta, Manish Goswami et. al., [3] suggests A Modified SRAM Based Low Power Memory Design. The suggested static random access memory (SRAM) design furnishes an approach towards curtailing the hold power dissipation. The design uses a tail transistor which aids in limiting the short circuit power dissipation by disrupting the direct connection between supply voltage and ground. This tail transistor also brings down the sub threshold current by providing stacking effect, which subsequently reduces hold power dissipation. A supply voltage of 0.8V is used which makes it eligible for low power applications.

J. Ramesh, P. Brundavani et. al., [4] presents a Design of Power Efficient High Performance SRAM Cell using Transmission Gates (TG). A TG primarily based 10T SRAM exploitation voltage swing cell at 0.09 um feature size in CMOS is planned to accomplish low power memory operation. This project compares proposed TG-VS SRAM cell with existing SRAM cells in terms of power and delay with different temperature . To implement proposed TG-SRAM cell in Tanner EDA (Electronic Design Automation) tool with 90nm CMOS environment is used.

Kolsoom Mehrabi, Behzad Ebrahimi and Ali Afzali-Kusha et. al., [5] suggests A Robust and Low Power 7T SRAM Cell Design. In this paper, we propose a new seven transistors (7T) static random access memory (SRAM) cell that improves read stability and write ability of the conventional 6T SRAM cell. Separating read and write access transistors in this cell solves the conflict of access transistor sizing. Therefore, large write and small read access transistors are chosen leading to read stability and write ability enhancement. Moreover, by isolating the storage node from the read path, more improvement in the read stability is achieved.

Ajay Gadhe, Ujwal Shirode et. al., [6] presents Read stability and Write ability analysis of different SRAM cell structures. This paper represents the simulation of three SRAM cell topologies and their comparative analysis on the basis of read noise margin (RNM), write noise margin (WNM). Both 8T SRAM cell and 9T SRAM cell provides higher read noise margin as compared to 6T SRAM cell. All simulations of the SRAM cell have been carried out in 130nm CMOS technology.

C. Ramya Shruthi, S.Rambabu, et. al., [7] Implements an Efficient SRAM for Ultra-Low Voltage Application Based on ST for Better Read Stability and Write Ability. In this paper we are going to propose a new SRAM bitcell for the purpose of read stability and write ability by using 90nm technology, and less power consumption, less area than the existing Schmitt trigger1 based SRAM. Design and simulations were done using DSCH (Dual Serial Channel) and Microwind.

Rajlaxmi Belavadi, Pramod Kumar.T, Obaleppa. R. Dasar, Narmada. S, Rajani. H. P et. al., [8] suggests Design and Implementation of Low Leakage Power SRAM System Using Full Stack Asymmetric SRAM. This paper explores the design and analysis of Static random Access Memory (SRAMs), focusing on optimizing delay and power. To address sub threshold leakage issue full stack approach is used. The full stack technique reduces leakage power to a great extent. The full stack technique is applied to SRAM cell in asymmetric manner in order to realize still higher power reduction. This work compares performance of SRAM

using full stack approach with that of conventional 6T-SRAM design.

A. Islam, M. Hasan et. al., [9] presents Leakage Characterization of 10T SRAM Cell. This paper presents a technique for designing a low-power and variability-aware SRAM cell. The cell achieves low power dissipation due to its series-connected tail transistor and read buffers, which offer a stacking effect. This paper studies the impact of process, voltage, and temperature (PVT) variations on most of the design metrics of the SRAM cell and compares the results with standard 6T, 9T, and ST10T (Schmitt trigger based) SRAM cells.

Yuan-Yuan Wang, Zi-Ou Wang; Li-Jun Zhang et. al., [10] suggests A new 6-transistor SRAM cell for low power cache design. This paper presents a new 6T-SRAM cell structure of nano-scale technology for low power application. Simulation results with standard 65nm CMOS (complementary metal oxide semiconductor) technology show that the speed is closed to the traditional 6T cell, power consumption is reduced by 22.45% during the write operation of 0. Particularly, in idle mode this structure maintains its data with the help of leakage current and positive feedback, which can greatly improves the power consumption of the nano-scale SRAM.

III. 7T SRAM MEMORY ARRAY IMPLEMENTATION WITH 28 NM TECHNOLOGY

In this section, a novel design and implementation of 7T SRAM array with 28 nm technology using SVL method is presented. The 7T SRAM cell incorporates seven transistors: five NMOS transistors, two of them are access transistors, two of them are employed to manufacture cross-coupled inverters, and one of which is paired with a feedback transistor, It has a similar architecture to a 6T SRAM cell, but it incorporates an additional NMOS circuit wired as a feedback transistor. A 6T Static random memory cell and an additional NMOS transistor Cell are included in the 7T SRAM array mobileular. This additional transistor is placed inside the floor direction for the reduction of leakage while the cellphone is in standby mode. Q, BLB (Bit Line Bar) and BL ((Bit Line) are alternatively charged and discharged, as well as the phrase wire throughout the additional transistor, to write 1 to the ground terminal output. One more PMOS transistor can be switched on, results 1 at qb, and q is charged to 0 through the NMOS transistor. Similarly if Q is 1 then Q' is 0.

The pre-charge circuit is a critical component that is used in an SRAM memory cell array construction, it's before we begin operations on the memory cell, our responsibility is to charge the bit lines BL, BLB to the greatest voltage possible., to achieve this we will be using a pre-charge circuit.

The speed of the row decoder has a great impact on memory performance. The row decoder drives the word lines of the SRAM array. At each read/write operation only one driver is active, making the SRAM cells connected to the corresponding word line accessible. The pulsed word line scheme (PWL) can be implemented by gating the outputs of standard decoders with a control enable pulse (from the sensing of voltage swings on the bit lines), which limits the duration of active output signals. Row and column decoders work together to pick a specific memory cell in the memory array. The row decoder is used to pick a specific row in the memory array that must be activated by connecting to the memory cell's world line.

During the read operation the voltage on one of the bit line or bit line/ will slightly start droping. A full swing on the line is

rather a slow operation. Hence, sense amplifiers are used to sense the slight voltage difference and amplify it to a correct data value. Additional stages can boost the speed of read operation significantly. It is used to read data from the cell and this operation has to be fast and accurate for the efficient working of the memory cell.

The Write Driver is responsible for writing data into memory. The driver's task is to get the BL and BLB towards the ground so that the alternate function may begin. Word Line (WL) enabled controls whether the Write Driver has access to the bit line. The term enable is used to allow the driver to work. It is divided into two NMOS transistors that are linked fascinatingly one after the other. To begin, two logics are assigned to the two points of the junction: 0 and 1. The bit line next to the 0 logic is discharged first, followed by a logic flip. As a result, the BL and BLB are discharged to the ground. Its main task is to keep a low connection to the ground.
The SVL technique is used to minimize the leakage power of the circuit. This circuit is operated in both operation modes which are Active mode and standby mode. a self-controllable voltage level (SVL) technique is proposed where the load circuits in active mode allows full supply voltage and decreased supply voltage appears to be proficient for reducing gate leakage currents as well. It generates power when the circuit is in an idle state. a low voltage and a comparatively high voltage "OFF MOSFET" decrease V sub through the "ON" control. As a result, Vth rises. As a result, the sub-threshold current falls. SVL circuits are classified into three types namely: Type 1 stands for upper SVL circuit, Type 2 stands for lower SVL circuit, and Type 3 stands for both combined. This technique is well suited for circuit in standby mode as leakage power is reduced more as compared to other techniques.

The Presented 7T SRAM array is designed and implemented with 28nm technology. The basic 8X8 Memory Array contains 64 bits of data. This SRAM array contains eight pre-charge circuits, eight write circuits in every column, Eight sensing amplifiers, and eight drivers in every row. A 3:8 Row decoder is employed to select a particular row. As a result, just one cell is active at any given time, allowing us to do certain tasks. The read and write operations of presented 7T SRAM array using SVM methods are as follows: the Fig. 1 shows the read operation of presented 7T SRAM array.

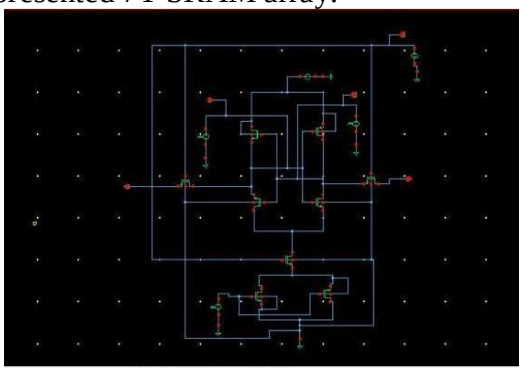

Fig. 1: THE 7T SRAM ARRAY USING SVL DURING READ MODE

To start the read operation, firstly the phrase line SRAM must be controlled and Memory must first contain some data. Consider memory with Q is 1 and memory with Q' is 0. Add a word line to the head of the line. If the available voltage across the node is Vdd 1, the bit and bit b output traces can be charged first. Because each Q and BL is too high, in the circuit, there is no discharge. If Q is 0, then there is a voltage divergence between "Q" and the terminal voltage at BL that drives the voltage at BL to collapse.

The circuit discharges as a result of the power passing through it. The BL and

BLB are combined with a sense amplifier. As of result, when the bit line is lower, then the result is Finally 1.

Let us use Q as 0 and Q' as 1 in the read operation. The word bit is remarkably high, allows to do write operations. Input lines for write operations are BL and BLB. Connect pin BL to the ground initially because we have command over the bit line. Thereby, a voltage divergence among qb and BL can be achieved. P1must be higher than P2 in addition to writing 1 to the Memory cell. This is accomplished by adjusting the ratio of the transistor. Finally, Q equals 1. Following the operation Q as 1, the first Q' as 0 occurs, followed by the Memorization success in the SRAM cell.

The metrics like power consumption, leakage power and leakage current of presented SRAM are analyzed.

IV. RESULT ANALYSIS

In this section, the result analysis novel design and implementation of 7T SRAM array with 28 nm technology using SVL method is demonstrated. A 7T SRAM array is designed and implemented with 28 nm technology. This 7T SRAM contains 8 sensing amplifiers, 8 driver circuits, eight pre-charge circuits and eight write circuits in its each row and column respectively. To choose a specific column/ row, a 3x8 decoder is used.

The performance of presented 7T SRAM array using SVL method is compared with conventional 7T SRAM array in terms of power consumption, current leakage and power leakage. The table 1 represents performance comparison of presented 7T SRAM using SVL and 7T SRAM array.

Table 1: PERFORMANCE COMPARISON OF PRESENTED 7T SRAM ARRAY AND 7T SRAM

Performance metrics	7T SRAM array	Presented 7T SRAM array using SVL
Leakage power (nW)	40.5nW	15.36nW
Leakage Current (nA)	60.75nA	23.47nA
Power Consumption (uW)	0.078 uW	0.0345uW

The Fig. 3 shows the power and current leakages comparison of general 7T and presented 7T SRAM using SVL method.

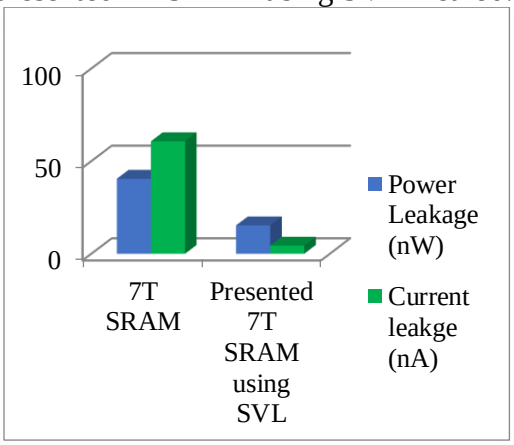

Fig. 2: PERFORMANCE COMPARISON OF 7T SRAM AND PRESENTED 7T SRAM ARRAY USING SVL METHOD

T
c
SRAM and Presented 7T SRAM array using SVL method.

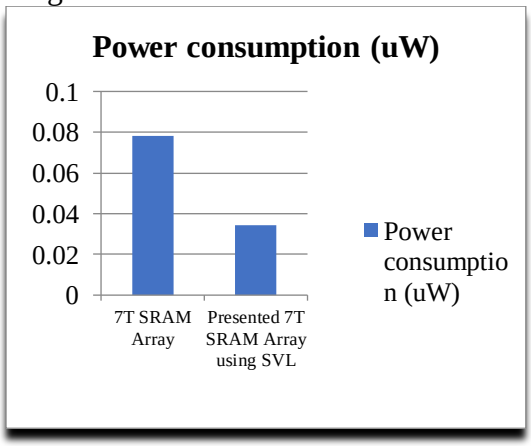

Fig. 3: COMPARATIVE GRAPH OF POWER CONSUMPTION

Therefore presented 7T SRAM Array using SVL method has better consumption of power, leakage power and leakage current than conventional 7T SRAM.

V. CONCLUSION

In this work, a novel design and implementation of 7T SRAM with 28 nm technology using SVL method is presented. Presented 7T SRAM array is fabricated through 28 nm technology. This presented 7T SRAM array mainly contains sense amplifiers, decoders, pre-charge circuits and write driver circuits. The Self-controllable Voltage Level (SVL) method is used to reduce the energy dissipation and this reduces the current leakage during transition modes and reduction in leakage current finally causes the reduction of power consumption of the proposed SRAM cell. The performance of presented 7T SRAM array is measured in terms of power consumption, current leakage and power leakage. The performance of presented 7T SRAM using SVL method is compared with conventional 7T SRAM array. From the results it is clear that compared to conventional 7T SRAM, presented 7T SRAM using SVL method has reduced power consumption, leakage power and leakage current. Hence presented 7T SRAM array is suitable for digital media applications.

VI. REFERENCES

[1] Beram Eswar Charan Teja, M. Damodhar Rao, Dr. Y. V. Narayana, Dr. V. V. K. D. V. Prasad, "Design & Implementation of Improved SRAM Cell", International Journal of Engineering Science and Computing, June 2017, volume 7, issue no.6, 2017 IJESC

[2] Pulla Reddy A, G Sreenivasulu, R Veerabadra Chary, "Write and Read Assist Techniques for SRAM Memories in Nanometer Technology", ICEMS 2016, Materials Today: Proceedings 4 (2017) 10309–10314, Elsevier

[3] Apoorva Pathak, Divyesh Sachan, Harish Peta, Manish Goswami, "A Modified SRAM Based Low Power Memory Design", 2016 29th International Conference on VLSI Design and 2016 15th International Conference on Embedded Systems (VLSID), DOI: 10.1109/VLSID.2016.80

[4]J. RAMESH, P. BRUNDAVANI, "Design of Power Efficient High Performance SRAM Cell using Transmission Gates", International Journal of VLSI System Design and Communication Systems Volume.04, IssueNo.08, August-2016, Pages: 0659-0663

[5] Kolsoom Mehrabi, Behzad Ebrahimi and Ali Afzali-Kusha, "A Robust and Low Power 7T SRAM Cell Design", 2015 18th CSI International Symposium on Computer Architecture and Digital Systems (CADS), 978-1-4799-5359-2/14, 2015 IEEE

[6] Ajay Gadhe, Ujwal Shirode, "Read stability and Write ability analysis of different SRAM cell structures", International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622, Vol. 3, Issue 1, January - February 2013, pp.1073-1078

[7]C.Ramya Shruthi,S.Rambabu, "Implementation of an Efficient SRAM for Ultra-Low Voltage Application Based on ST for Better Read Stability and Write Ability", IOSR Journal of Electronics and Communication Engineering (IOSR-JECE) e-ISSN: 2278-2834,p- ISSN: 2278-8735. Volume 6, Issue 4(May. - Jun. 2013), PP 56-61

[8] Rajlaxmi Belavadi, Pramod Kumar.T, Obaleppa. R. Dasar, Narmada. S, Rajani. H. P, "Design and Implementation of Low Leakage Power SRAM System Using Full Stack Asymmetric SRAM", International Journal of Advanced Research in

Electrical, Electronics and Instrumentation Engineering Vol. 2, Issue 7, July 2013, ISSN (Online): 2278 – 8875
[9] A. Islam; M. Hasan, "Leakage Characterization of 10T SRAM Cell", IEEE Transactions on Electron Devices (Volume: 59, Issue: 3, March 2012) DOI: 10.1109/TED.2011.2181387
[10] Yuan-Yuan Wang, Zi-Ou Wang; Li-Jun Zhang, "A new 6-transistor SRAM cell for low power cache design", 2012 IEEE 11th International Conference on Solid-State and Integrated Circuit Technology,DOI: 10.1109/ICSICT.2012.6467902