Journal of Advanced Research in Technology and Management Sciences
Volume: 01 Issue: 03 ISSN: 2582-3078 November 2019
Available online at: http://www.jartms.org

SURVEY ON PHASE LOCKED LOOP AND DIGITAL PHASED LOCKED LOOP

[1]GUVVALADUNNE PRASANNA KUMAR, [2]Dr VIJAY PRAKAH SINGH
[1]Research scholar, Sri Satya Sai university of Technology & Medical Science, Sehore, Bhopal, Madhya Pradesh, India
[2]Research Guide & Associate professor, Sri Satya Sai university of Technology & Medical Science, Sehore, Bhopal, Madhya Pradesh, India

ABSTRACT: Phase Locked Loop (PLL) is a closed loop, negative feedback system. A closed-loop feedback control system, which synchronizes its output signal in frequency as well as in phase with an input signal, is PLL. The phase detector, loop filter, and the voltage controlled oscillator are the key parts of almost all PLLs. This paper gives investigation study of various PLL works suggested by some researches for low power and performance applications. Also, an attempt of understanding different technologies and reviewing the different methods of designing a low power PLL has been made. In this paper survey on different types of Phased locked loop techniques for low power and high performance applications is presented. Firstly the general structure of PLL is explained briefly then some of the PLL techniques which are focused on low power and high performance can be studied. Then all circuits that are studied will be compared and a result analysis can be performed. From the result analysis it can be found that the Digital Phased Locked Loop (DLL) have result in good phase noise performance with low power consumption with improved tuning range as compared to other phased locked loop circuits, as it uses the CMOS technology providing the real solution in the band of radio frequency. It is used in various applications such as wireless sensor network, transceiver, Clock generations, clock recovery circuits etc.

KEY WORDS: Phase Locked Loop (PLL), phase detector, loop filter, voltage controlled oscillator (VCO), Digital phased locked loop (DLL).

I. INTRODUCTION

In synchronous digital circuits, require a signal that oscillates between a high and a low state and is used to coordinate actions of circuits which is known as clock signal. A clock signal is generated by a clock generator using a crystal. In general the clock signal is a square wave with a 50% duty cycle, usually with a fixed, constant frequency [1]. Many modern microcomputers use a "clock multiplier" which multiplies a lower frequency external clock to the appropriate clock rate of the microprocessor [2]. This allows the CPU to operate at a much higher frequency than the rest of the computer, which affords performance gains in situations where the CPU does not need to wait on an external factor (like memory or input/output). However, PLLs require much time and design efforts to ensure stability. And also PLLs consume large silicon area and often require different external components for usage, resulting in high cost. Because of high lock time of PLL, the input clock signal frequency cannot be changed quickly. PLLs are only suited for handling input clock signals of limited frequency and duty cycle ranges [3].

Phase locked loop is abbreviated as PLL. Brain of phase locked loop is voltage controlled oscillator. In technical fields, such as frequency control, frequency synthesizing, FM (frequency modulation) demodulation, data recovery, signal synchronization, are used PLL [4]. Jitter attenuator for reduce noise within jitter is the versatile application of the phase locked loop that is for communication system, networking and variation of phase is carried on a clock signal. Phase locked loop circuit is necessary for increasing circuit speed. This is known to provide a clock recovery circuit using a phase locked loop for example, in a digital transmission system, a clock signal which is used for timing purposes in processing the data signal [5]. The data signal is a serial binary signal having binary 0s and 1s represented respectively by the absence and presence of a positive voltage and the clock signal is produced at the bit rate of the

data signal. The present innovation relates to a phase-locked loop, and more particularly, to frequency stabilization of an oscillation output signal generated by a phase locked loop [6].

In recent development era, new involvement of emerging technologies vastly introduced in the field of VLSI. This study is based on PLL which is started in early in 1932 which reach to its peak with a great upsurge whereas consumption of power and circuit area is reduced [7]. By appropriately choosing the Phase frequency detector framework and adjusting the charge pump current and the loop filter design values can be achieved a better lock time. Many researchers have undertaken different techniques for designing PLL and its components. Most of the researchers have carried out the research work in the view of increasing frequency or reducing parameters such as area, power consumption, jitter, phase noise etc. Various researchers have presented papers on low power PLL design by modifying the design of various PLL components and parameters like supply voltage, threshold voltage, etc.

II. PHASE LOCKED LOOP (PLL)

A PLL is characterized by the frequency range, jitter, jitter attenuation and lock time. PLLs are only used for generation of high frequency stable clocks and are normally feed by quartz controlled oscillators so that there is no need for jitter attenuation [9]. The Phase-Locked Loops (PLLs) are probably the most widely used synchronization technique in grid-connected applications. The key feature of open-loop synchronization techniques is that they are un-conditionally stable. Fig. 1 shows the basic structure of PLL. Among the various synchronization techniques, PLLs have found much attention, mainly due to their simplicity, robustness, and effectiveness. A PLL is a closed-loop feedback control system, which synchronizes its output signal in frequency, as well as in phase, with an input signal [10]. With the advanced technology of microcontrollers and Digital Signal Processors (DSPs), all of the functions of the classical PLL have been implemented by software. The components are:

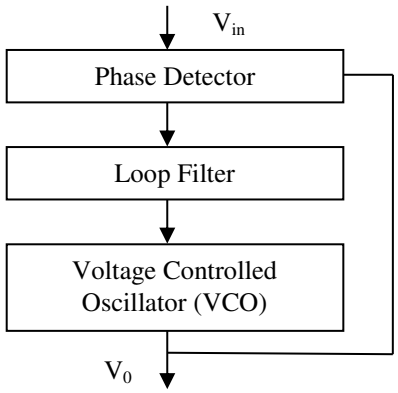

Fig. 1: BASIC PLL STRUCTURE

2.1 Phase and Frequency Detector

The first component in PLL is the Phase and Frequency Detector (PHD). The output of the PFD depends on both the phase and frequency of the inputs. This type of phase detector is also termed a sequential phase detector. It compares the leading edges of data and data1 (data is the input signal to PFD, data1 is considered as the feedback signal from the output of VCO to PFD) [11]. A data1 rising edge cannot be present without a data rising edge. If the rising edge of the data leads the data1 rising edge, then the up output of the phase detector goes high while the down output remains low. This causes the data1 frequency to increase and makes the edges move closer. If the data1 signal leads the Data up remains low while the down goes high then the phase difference between data1 and data can be found.[12].

2.2 Loop Filter

The second component in PLL is the loop filter. The loop filter consists of two parts, the charge pump and the RC filter. The output of the PFD should be combined into a single output to drive the loop filter. In charge pump, two NMOS and two PMOS are connected serially. The uppermost PMOS and lowermost NMOS are considered as the current source and the other PMOS and NMOS in the middle are connected to the up and down of the output of PFD [13]. When the PFD up signal goes high, the PMOS will turn on. This will connect the current source to the loop filter. It is in the similar way when the PFD down signal goes high. The loop filter is a simple RC filter. However, it plays a very important role in the PLL [14]. Unless the loop filter values are correctly chosen, it would take the loop too long to lock or once locked it is still unstable small variations in the input data may cause the loop unlock again. If the rising edge of data leads that of data1, then the PFD up goes high. And it will cause the voltage of the output signal of the loop filter become higher. If the rising edge of data lags that of data1, the PFD down goes high. It would cause output signal of the loop filter become lower.

1.3 Voltage Controlled Oscillator

In the voltage controlled oscillator (VCO), the main part is the multiple stage oscillators which are similar to the ring oscillator. In each stage, there are two PMOS and two NMOS. The upper most PMOS and lower most NMOS operate as current source and the PMOS and NMOS in the middle operate as inverter. The current sources limit the current available to the inverter. Compared with the resistance and capacitance present in the loop filter, the resistance of the VCO should be designed infinite and the capacitance of the VCO should be designed smaller [15].

III. SURVEY ON PLL AND DLL TECHNIQUES

Many researchers have undertaken different techniques for designing PLL and its components. Most of the researchers have carried out the research work in the view of increasing frequency or reducing parameters such as area, power consumption, jitter, phase noise etc. Various researchers have presented papers on low power PLL design by modifying the design of various PLL components and parameters like supply voltage, threshold voltage, etc.

3.1 A Low Power Sub-GHz PLL with Optimized LO Distribution Circuit

In this paper, a delta sigma fractional frequency synthesizer with an optimized LO distribution circuit is presented to work at sub-GHz ranges. It is able to provide drive to the RF transceiver with low power consumption. A wideband fractional-N Phase-Lock Loop (PLL) is designed for sub-GHz wireless communications. The Local Oscillator (LO) distribution circuit is optimized with a low power consumption and high output amplitude to drive the mixer and power amplifier of the transceiver.

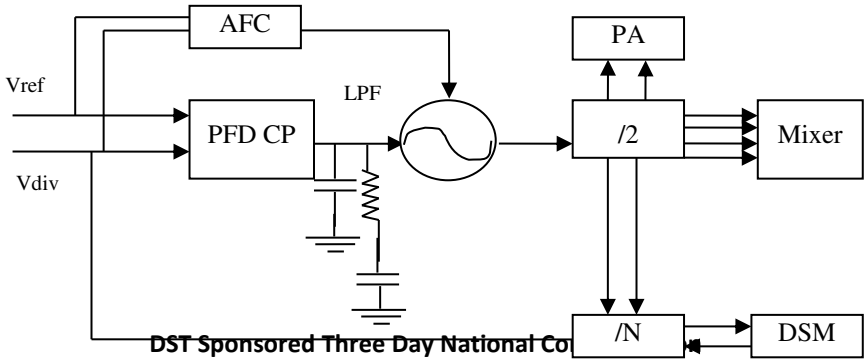

Fig. 2: BLOCK DIAGRAM OF FREQUENCY SYNTHESIZER

Fig. 2 shows the block diagram of presented frequency synthesizer. The overall circuit consists of eight parts, namely the adaptive frequency calibration circuit (AFC), Voltage-Controlled Oscillator (VCO), divide-by-N divider circuit, Delta Sigma Modulator (DSM), Phase Frequency Detector (PFD), Charge Pump (CP), Low Pass Filter (LPF) and LO distribution circuit as illustrated with the red rectangular. The detailed topology of the LO distribution circuit is much more complex which not only contains pre scalar, but also has differential to single-ended circuit and a series of buffers. The design of high-speed blocks is carried out as follows. Firstly, the wideband VCO is designed with continuous frequency tuning and the capacitor array is used for coarse calibration. Secondly, a conventional DSM is designed to generate the fractional part of division ratio. An almost consequent locking range can be realized with the fractional divider. Besides, AFC is used to help PLL achieving fast locking. As shown in block diagram, the main component of the LO distribution circuit is divide-by-two unit, which consequently provides signals for PA, mixer and divide-by-N divider in PLL system. Since the VCO is designed to run at twice of the target frequency, the divide-by-two divider works as a pre scalar and output buffer, which is implemented with the current mode logic (CML). A series of buffers and other functional blocks are designed because the signal required by each component is quite different. The input of mixer is quadrature signal while the inputs of PA and divide-by-N divider are differential signals. Besides, the input impedance of each component is different, and the LO distribution circuit should satisfy the inter-stage matching. In order to satisfy balanced load for CML divider, a four-channel buffer is connected right after CML divider. After the divider, LO signal is then distributed to three different routes. A differential to single-ended transfer buffer is added before PA as only needed single-ended signal.

3.2 PLL for Fast Phase and Frequency Acquisition

This paper presents a PLL with designing of each block to achieve fast locking time with reduced power consumption, less jitter and phase noise. This paper presented a PLL with redesigning of individual blocks. The block diagram of this PLL is shown in Fig. 3, it compares the output signal with the input signal. The comparison is performed by a phase frequency detector. The basic building blocks of a Phase locked Loop (PLL) are Phase Frequency Detector (PFD), Charge Pump (CP), Low Pass Filter (LPF) and Voltage Controlled Oscillator (VCO) in a feedback loop through a frequency divider.

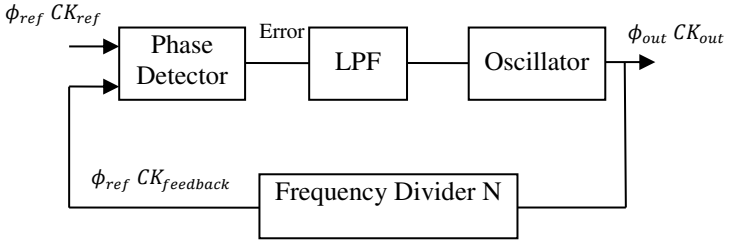

Fig. 3: BLOCK DIAGRAM OF PHASE LOCKED LOOP

The role of phase frequency detector is to generate a digital signal (difference or error signal) that drives the charge pump to either increase the control voltage of the VCO or decrease it or keep it without change. PFD compares the phase and frequency of two input signals and generates an error signal which is proportional to the phase deviation between them. It detects both phase and frequency differences. If there is a phase difference between the two signals, it generates “UP” or “DOWN” synchronized signals. The Charge pump circuit converts the

phase or frequency difference information into a voltage. It is used to combine both the outputs of the PFD and give a single output which is fed to the input of the filter. The low pass filter converts undesirable high-frequency (ac) components to desirable dc components. Thus, provides a steady control voltage or the dc level to operate the VCO. The voltage controlled oscillator is the circuit block where the control voltage of CP controls the oscillator's output frequency so that it matches the reference signal frequency. This VCO output frequency is divided by the divider N. It scales down the frequency of the VCO output signal. The output of the VCO has to be divided before it is fed back to the input of the PLL. It divides the reference clock signal by N and provides an output pulse signal for every N cycles of reference clock signal.

3.3 A Fully Synthesizable All-Digital Phase-Locked Loop

This paper presents an All-Digital Phase-Locked Loop (ADPLL) design method based on standard cells. A new portable architecture is introduced. Its motor is a fully synthesizable description of a Digital Controlled Oscillator (DCO) with Variable Length Ring Oscillator (VLRO) as coarse part and fine-tune unit based on path selector of different pin-to-pin delays in NAND standard cell. Time to Digital Converter (TDC) circuit with a two level structure has been added to reduce the oscillator frequency's initial coarse-tune time. TDC allows finding the desired output frequency in two reference clock cycles. The two level structures reduce the hardware implementing costs of this block. The circuit is designed using standard library cells only and is described in Verilog HDL. This enables design automation and simplifies the design of digital signal processing circuits for modern System-on-a-Chip. The general definition of digital PLL includes both all-digital PLLs and intensive digital systems. In intensive digital PLL systems, all input and output signals for each PLL module are digital, but the module may contain an analog function. An example would be an implementation where a digitally controlled LC-tank is used as an oscillator. The architecture of ADPLL is similar to an analog PLL. The analog filter and charge pump are replaced by a digital loop filter and a digital controller, and the VCO is replaced by a DCO (Figure 4).

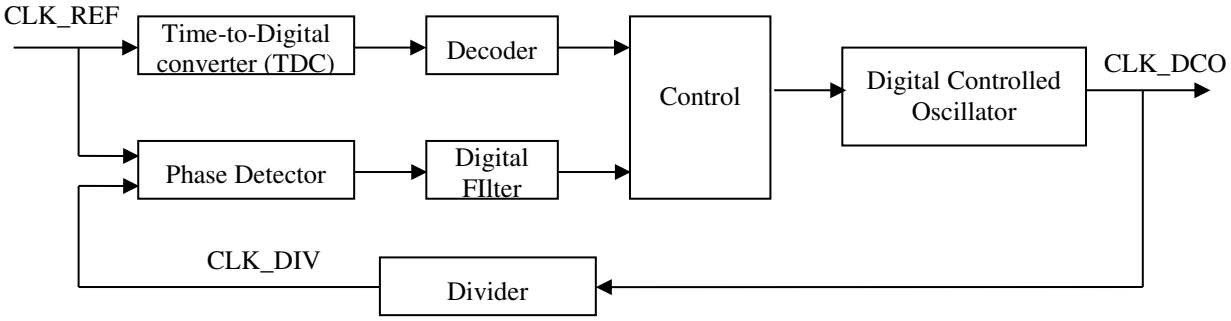

Fig. 4: ADPLL TOP LEVEL

To reduce the synchronization time, a TDC is added. The TDC is used to convert time information about the input reference signal into a digital code. TDC provides the controller information about a period length of the input reference signal. A delay on standard digital library cell is used as a timing scale unit. Controller process the TDC output code to the Coarse-Tune Word (CTW) and starts the oscillator at the required frequency. Next, the controller's state machine puts the PLL in phase acquisition mode to fine-tune the frequency. DCO is the key difference between all-digital PLLs versus analog and intensive digital ones. It is designed using only digital components. DCO works with digital inputs and digital outputs in the discrete-time domain. To reduce the output frequency tuning step and increase the accuracy of searching for the target value, a DCO was presented with coarse and fine frequency control.

3.4 Low-Power Linear SAR-Based All-Digital Delay-Locked Loop

This paper presented a500 MHz to 1.5 GHz 8-bit SAR-based All-Digital Delay-Locked Loop (ADDLL) design and simulation in a 130 nm CMOS technology. This ADDLL employs a novel Digitally Controlled Delay Line (DCDL), which presents a good linearity for the SAR code-delay curve and low power consumption. Compared to other SAR-based ADDLLs, there is no complex binary to thermometer decoder in the presented DCDL that leads to low power dissipation and small area. In order to track PVTL variations, once the ADDLL locks, the SAR controller circuit is converted into a counter.

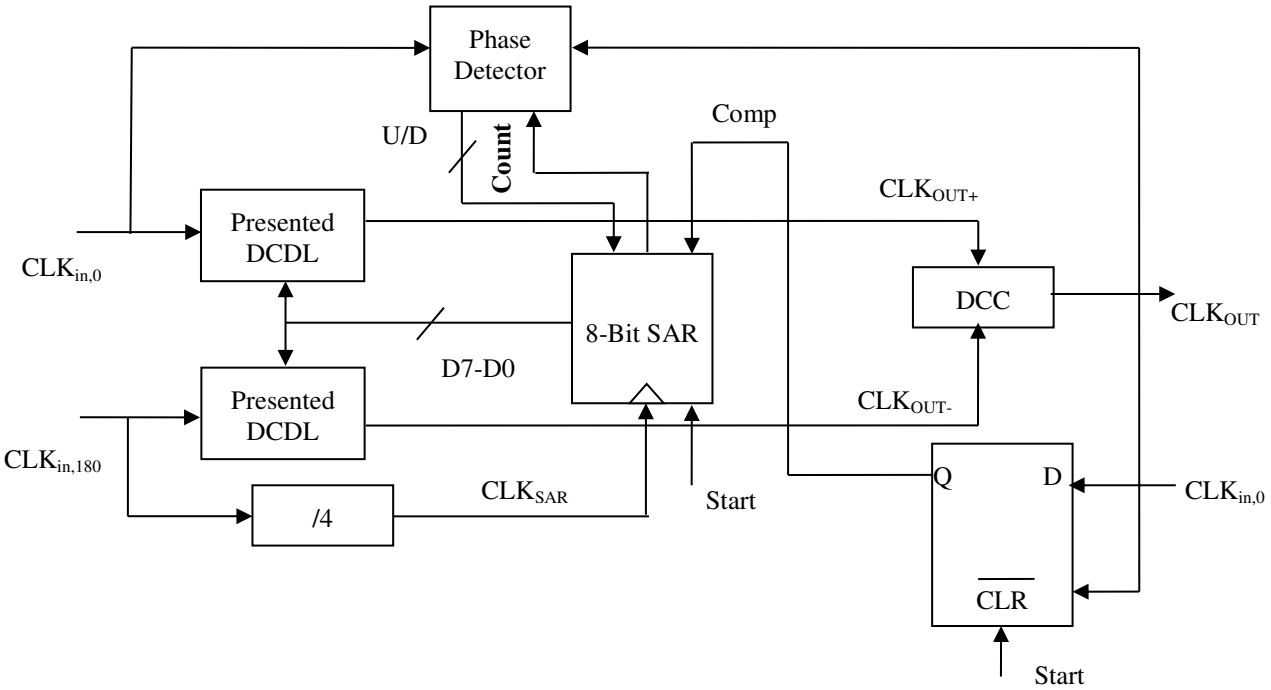

Fig. 5: BLOCK DIAGRAM OF THE PRESENTED SAR-BASED ADDLL

The SAR-based all-digital DLL is shown in Fig. 5. This DLL consists of two DCDLs, an 8-bit SAR controller circuit, a digital phase detector, a frequency divider, a Duty Cycle Corrector (DCC) and a D-type Flip-Flop (DFF) as a sampler. When the Start signal goes to logic one, then binary search begins. At first, the Most Significant Bit (MSB) is logic one and the other bits stay at zero. With the first rising edge of the CLK_{SAR}, the control SAR code changes the delay of DCDLs and the delayed signals CLK_{OUT+} and CLK_{OUT-} are merged by the DCC circuit and generate CLK_{OUT}. CLK_{IN0} and $CLK_{OU}T$ are compared by the sampler and according to the output of the sampler the MSB stays logic one or goes to zero. The binary search continues until all of the control bits are specified. When the binary search is complete, the stop signal arises and the SAR controller converted into an 8-bit counter for closed-loop operation. At the end, the signal stop goes to logic one in order to activate the digital phase detector to track PVTL variations. The SAR unit consists of a number of logic gates that determine each one of the control bits according to the input control signals. While the signal Enable is logic one, the signals Shift and Comp are ignored and the signals U and D decide the output of the SAR units. The Digitally Controlled Delay Line (DCDL) consumes most power and chip area in an ADDLL and its code-delay curve linearity is one of the important

features that need to be considered. The DCDL consists of a Coarse Delay Line (CDL) and a Fine Delay Line (FDL).

IV. RESULTS

4.1 A Low Power Sub-GHz PLL with Optimized LO Distribution Circuit

The most critical part of LO distribution circuit is divide-by-two frequency divider and the first stage of the buffer as their operation frequency is the highest in LO distribution circuit. The tail transistor in CML divider is biased near cut-off region to reduce power consumption. Meanwhile, CMOS inverter buffer is used rather than CML buffer as CMOS buffer is much more power efficient. To further reduce power consumption, cascaded inverters are employed at the first stage of buffers. Cascaded inverter employs charge reusing technique reducing inverter stages which reduce branch current expenditure. Moreover, the cascaded structure restricts the output amplitude which is beneficial in reducing power consumption. In that case, almost half power consumption can be saved as well as silicon area is reduced. In the whole PLL system, the most area-costing devices are the inductor and capacitor. In that case, inductor of VCO and LPF are implemented off-chip to save silicon area. Besides, it's also impossible to move coupling capacitor off the chip as their distribution is quite separate and the capacitance is comparable to parasitic capacitance of bonding lines and PCB. In that case, the AC-coupling capacitors should be properly sized to reduce area as small as possible while satisfying system requirement simultaneously. The layout and die microphotograph of PLL system were performed. The area of PLL core without pads is 782μmx423μm. Vref, the input reference signal, is connected to 10MHz signal generator in measurement. Since inductor of VCO and LPF are moved off the chip, they are added in PCB in measurement. Among them, vcon and vcop signals are the two ports of off-chip inductor. The output spectrum is measured while the PLL system is locked. The frequency of VCO output is 1.26GHz with -15.06dBm amplitude corresponding to 630MHz after the divide-by-two unit. The static power consumption of PLL is 3.5mW including all the buffers.

4.2 PLL Design for Fast Phase and Frequency Acquisition

To achieve good PLL performance a charge pump is presented that has some characteristics; increased output voltage, show charging waveform when UP signal is high and discharging when DOWN signal triggers high, Low Power consumption. Thus by combining all the individual blocks such as frequency divide-by-2, VCo and frequency divider, a PLL was acquired with the properties of very less locking time, low power consumption, less delay, reduced phase noise, less Jitter. In this paper, the fast locking and low power PLL has been designed and simulated using Gpdk 180 nm technology of cadence tool for analysis of phase and frequency. For these specific properties of PLL a charge pump of current mirrored power consumption is used with appropriate parameters of PFD, LPF and VCO. Thus the PLL is designed with a very less locking time of 250.6ns and it is observed a power consumption of 11.0mW.

4.3 A Fully Synthesizable All-Digital Phase-Locked Loop

The ADPLL was described in Verilog HDL and synthesized to CMOS 90nm library. The core area is 150μm x 450μm. TDC occupies 70 percent of all core area, DCO - only 10 percent. The ADPLL lock range is 100-292 MHz with a 10MHz reference frequency at 1.2V. The division ratio is 16. Thus, the output frequency is 160MHz (=10MHz * 16). The TDC takes two reference clock cycles to complete fast coarse frequency search operation. After TDC operation is completed, the controller fixes CTW code on DCO and Phase Detector begin

control phase acquisition by changing FTW code on DCO. Table 1 shows a comparison with previously reported researches ADPLLs. Presented circuit shows good results in terms of lock-in time and small area.

4.4 Low-Power Linear SAR-Based All-Digital Delay-Locked Loop

The ADDLL was designed and simulated in a 130 nm CMOS technology using Cadence. Based on the SAR code-delay curve of the presented DCDL, the ADDLL can work perfectly from 500 MHz to 1.5 GHz. The locking time is 32 clock cycles at all working frequencies. The total power consumption of the presented ADDLL is 1.15 mW at 1.5 GHz input clock frequency. Table 1 shows a performance summery and comparison between the presented ADDLL and previous SAR-based approaches. In this table the main characteristic such as frequency range, DCDL resolution, power consumption, etc. are compared. As shown in Table 1, there is a trade-off between power consumption and frequency range. As the frequency range increases, power consumption increases too. This article emphasizes on low power consumption.

The study of various research papers and investigations shows that usage of low power supply, power consumption, high performance in the design of low power PLL and DLL. Table 1 shows the comparison made by using the result analysis of four works presented in the survey. Traditionally a PLL is made to function as an analog building block, but integrating an analog PLL on a digital chip is difficult. Analog PLLs are also more susceptible to noise and process variations. Digital PLLs allow a faster lock time to be achieved and are attractive for clock generation on high Performance microprocessor.

Table 1: PERFORMANCE ANALYSIS OF SURVEY PAPERS

Parameter	LL with Optimized LO [16]	PLL [17]	ADPLL [18]	ADDLLs [19]
Frequency	0.3~1.286GHz	100MHz	100.8-292.4MHz	500MHz-1.5GHz
Supply Voltage	1.2V	1.8V	1.2V	1.2V
Power	3.5mW	11.0mW	-	1.15mW
Technology	0.13μm	180nm	90nm	130nm
Lock time	-	280.6nsec	<10cycles	32cycles

V. CONCLUSION

PLL is a closed-loop feedback control system that synchronizes its output signal in frequency as well as in phase with an input signal. Phase Locked Loops (PLL) circuits are used for frequency control. The Phase Locked Loop (PLL) is a very important and common part of high performance micro processors. In this paper a survey is done on various trends in Phase Locked Loop techniques. This paper first explained how PLL increase in technology day by day. Three components that are needed to make a PLL design which is phase detector, loop filter, VCO are studied. Then different PLL techniques are studied. At the end it was concluded from the result analysis that the Digital phased locked loops have result in good phase noise performance with low power consumption with improved tuning range as compared to other phased locked loop circuits. Phase locked loop have vast application like communication, networking, control system and also in daily life.

VI. REFERENCES

[1] H. Wu et al., "A method to transform synchronous pipeline circuits to bundled-data asynchronous circuits using commercial EDA tools", IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), pp. 1-2, 2019.
[2] N. Srivastava and R. Manohar, "Operation-Dependent Frequency Scaling Using Desynchronization", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 27, no. 4, pp. 799-809, 2019.
[3] Kailuke, Aniruddha & Agrawal, Pankaj & Kshirsagar, R.V., "Design of Low Power, Low Jitter PLL for WiMAX Application in 0.18µm CMOS Process", in Procedia Computer Science, 2019, pp 390-397.
[4] Xuefan Jin, Dong-Seok Kang, Youngjun Ko, Kee-Won Kwon, Jung-Hoon Chun, "A 4-GHz Sub-harmonically Injection-Locked Phase-Locked Loop with Self-Calibrated Injection Timing and Pulse width", IEEE Asian Solid-State Circuits Conference (A-SSCC), 2019
[5] H. Peng, R. Guo, Y. Xu, H. Du, J. Chen and Z. Chen, "Ultra-Low Phase Noise and Frequency Agile X-band Frequency synthesizer Based on a Phase Locked Optoelectronic Oscillator", Proceedings of the 2019 Joint Meeting of the IEEE Int. Fre. Control Symp. and the Eur. Fre. and Time Form, 2019.
[6] Y. Lee, T. Seong, S. Yoo and J. Choi, "A low-jitter and low-reference-spur ring-VCO-based switched-loop filter PLL using a fast phase-error correction technique", IEEE J. Solid-State Circuits, vol. 53, no. 4, pp. 1192-1202, Apr. 2018.
[7] D. Liao, F. F. Dai, B. Nauta and E. A. M. Klumperink, "A 2.4-GHz 16-Phase Sub-Sampling Fractional-N PLL With Robust Soft Loop Switching", IEEE Journal of Solid-State Circuits, vol. 53, no. 3, pp. 715-727, March 2018.
[8] S. Huang et al., "Low-noise fractional-N PLL with a high-precision phase control in the phase synchronization of multichips", IEEE Microw. Wireless Compon. Lett., vol. 28, no. 8, pp. 702-704, Aug. 2018.
[9] W. El-Halwagy et al., "A 28-GHz quadrature fractional-N frequency synthesizer for 5G transceivers with less than 100-fs jitter based on cascaded PLL architecture", IEEE Trans. Microw. Theory Techn., vol. 65, no. 2, pp. 396-413, Feb. 2017.
[10] Ghaderi, Noushin & Erfani-Jazi, Hamid & Mohseni, Mehdi. (2016), "A Low Noise, Low Power Phase-Locked Loop, Using Optimization Methods", in Journal of Electrical and Computer Engineering 10.1155/2016/8202581, 2016
[11] S. Golestan, F. D. Freijedo, A. Vidal, J. M. Guerrero, and J. Doval-Gandoy, "A quasi-type-1 phase-locked loop structure," IEEE Trans. Power Electron., vol. PP, no. 99, pp. 1-7, Jun. 2014.
[12] C. Hsu, K. Tripurari, S. Yu and P. R. Kinget, "A Sub-Sampling-Assisted Phase-Frequency Detector for Low-Noise PLLs With Robust Operation Under Supply Interference", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 62, no. 1, pp. 90-99, Jan. 2015.
[13] Davide Tasca, Marco Zanuso, Giovanni Marzin, Salvatore Levantino, Carlo Samori and Andrea L. Lacaita, "A 2.9-4.0-GHz Fractional-N Digital PLL With Bang-Bang Phase Detector and 560-fsrms Integrated Jitter at 4.5-mW Power," IEEE Journal of Solid-State Circuits, vol.46, no.12, pp.2745-2758, Dec 2011.
[14] A. Axholt and H. Sjöland, "A PLL based 12 GHz LO generator with digital phase control in 90 nm COMS", Analog Integr. Circuits and Signal Process., vol. 67, no. 3, pp. 309-318, Jun. 2011.
[15] S. Lee, S. Amakawa, N. Ishihara and K. Masu, "Low-phase-noise wide-frequency-range ring-VCO-based scalable PLL with sub harmonic injection locking in 0.18µm CMOS", Microwave Symp. Digest (MTT), vol. 11, pp. 78-1181, 2010.

[16] Lingchang Chen, Xiaopeng Yu, Hanqi Gao, Liying Cai, Kai Huang, Dandan Zheng, "A Low Power Sub-GHz PLL with Optimized LO Distribution Circuit", IEEE Xplore, 2020
[17] S.Anjaneyulu, J.Sreepavani, K.Pramidapadma, N.Varalakshmi, S.Triven, "Phase Locked Loop Design for Fast Phase and Frequency Acquisition", International Research Journal of Engineering and Technology (IRJET), Volume: 03 Issue: 04, April-2016
[18] Rustam Khalirbaginov. "A Fully Synthesizable All-Digital Phase-Locked Loop with Parametrized and Portable Architecture", EEE Conference of Russian Young Researchers in Electrical and Electronic Engineering (ElConRus), 2021
[19] Mohammadreza Esmaeilpour Quchani, Mohammad Maymandi-Nejad, Design of a Low-Power Linear SAR-Based All-Digital Delay-Locked Loop", 27th Iranian Conference on Electrical Engineering (ICEE2019), 2019