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DESIGN AND IMPLEMENTATION OF HIGH SPEED HYBRID ADDER WITH REVERSE CARRY PROPAGATE ADDER

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ABSTRACT:

This paper helps us to discuss about approximate Reverse Carry Propagate Adder (RCPA), In RCP adders the carry signal propagates in counter down flow manner. I.e. it flows from the maximized prioritized bit to the least prioritized bit. Henceforth the carry i/p signal has the greater significance then the o/p carry. This way of carry propagation increases the steadiness in presence of delay versions, here in this paper we are discussing about the three different designs of RCPA cells with different delay, energy, and accuracy configurations, and also we use a few hybrid structure within the n bit adder design were least half of the adder design is carried out with this RCPA and most considerable half will be introduced by way of using some accurate high pace adder like KoggeStone adder that may decorate the adder speed. The Hybrid adders realized utilizing those systems are studied and as compared people with conventional approximate adders with Xilinx ISE 14.7 Verilog HDL coding.

Keywords: Approximate adder, Digital Signal Processing (DSP), Reverse Carry Propagate adder (RCPA), Kogge Stone adder (KSA)

I. INTRODUCTION

Adder blocks, which are probably the precept additives in arithmetic devices of DSP systems, are electricity hungry and frequently form hot-spot locations on the die. The ones facts were the motivations for understanding this factor the usage of the approximate calculating approach. Early researches on approximate adders have taken state-of-the-art procedures of that specialize in errors weight and blunders opportunity reductions. Power intake reduction and pace development are the important thing dreams within the layout of digital processing units, specially the portable structures. Normally, a growth inside the speed is carried out at the value of greater power intake for actual processing units. One of the procedures to improve both the energy and pace is to sacrifice the computation exactness. This approach, which is approximate computing, may be used for the applications in which a few mistakes maybe tolerated. The first technique is primarily based on a hybrid shape adder where in two different components, actual MSBs & LSBs are utilized. Within the carry i/p of the MSB element and summation of the LSB component the error occurs. Consequently this reduces the error weight to the load of the carry i/p of the MSB part. Given that usually maximum of the activities get up within the LSB. Inside the second approach, natural approximate adder systems are employed. For those adders, reducing the error possibility of the summation further decreases the strength and delay which are the important things in layout criteria. As per the flow of this paper, we have recognized that the Hybrid Adders in which the use

of the approximate Reverse Carry Propagate complete-adder (RCPFA) is usually suggested. The approximate summing circuit propagates the i/p carry signal in a counter-down manner, i.e., from the higher remarkable bit to lower remarkable bit to form the bring o/p. on this form of adder this is known as Reverse Carry Propagate adder (RCPA) the propagation is finished via introducing a forecast signal appearing as an o/p signal, due to the alternative/opposite propagation, the weight of the carry decreases because it propagates. The MSB half of could be added with the assist of parallel prefix adder that can have better velocity of operation. Decrease component might be brought with the assist of approximate opposite carry propagate adder.

The structure of the paper is prepared as follows: In sector II we come across some related works which are briefly reviewed. Various designs of the proposed RCPFA are defined in sector III. The proposed approximate n-bit adder is proposed with approximate FAs in section IV. In section V we present the evaluation outcomes between proposed and current adder designs. Finally in section VI we conclude the paper

II. EARLIER WORK

Ripple carry adder (RCA) has the lowest strength and area usage amongst all the precise adder structures, but it suffers from a huge delay. To enhance the velocity and electricity efficiency of this adder, some earlier works have sacrificed the accuracy. An approximate RCA shape which is also known as Error Tolerant adder structure (EAS) has been provided. The shape of EAS is shown in Fig. 1. On this structure, the i/P operands are divided into components known as precise computation part and inexact computation element. Within the real aspect is the MSB part, the traditional FAs with a zero carry i/p for the whole component are used while the inexact part is the LSB element which includes a carry-free addition element.

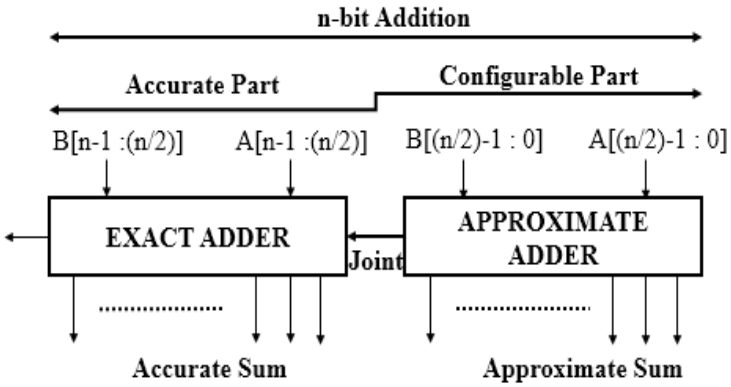


Fig.1 Error tolerant adder structure

Designing an adder with carry propagation will take more delay so if we avoid the carry propagation even as designing an adder will outcomes the better adder performance so we move for Reverse Carry Propagate adder in which the carry is propagated in contrary course. The formal full adder that's the necessary factor building block of the carry propagates adders has 3 i/ps with the identical weight. Moreover, it's outputs for a addition results with constant weight as that of the i/ps and a carry o/p with

times the load. The carry propagation delay (t_CP) is that the most essential timing parameter in associate full adder because of the truth that it determines the delay of the very important path of multi bit adders (and multipliers).

A small short-delay violation to boot additionally bring on a colossal quantity of errors because of the reality that the error takes region at the MSBs of the summation. That's the top results of the time and propagation of the carry i/p of the MSBs through tiny monumental bit FAs. Primarily based all during this reasoning, if the order of the carry propagation is reversed, one may expect that the amount of errors because of the timing violation decreases.

Reverse Carry Propagate Full-Adder Cell

Every specific FA generates its carry o/p and sum indicators the usage of

$$2C_{i+1} + Si = Ai + Bi + Ci \dots\dots\dots\dots (1)$$

Where $Ai(Bi)$ is the $i\text{^}th$ bit of the i/p $A(B)$, $Ci(Ci+1)$is the carry i/p, and Si is the $i\text{^}th$ bit of the sum. Based in this equation, the o/p signal within the $i\text{^}th$ bit role relies upon on the $i\text{^}th$ bits of the i/p's A&B and the deliver o/p of the preceding function (Ci). Via shifting the term Ci $(Ci+1)$ to the left (right) aspect of the equation, one may additionally write

$$Si - Ci = Ai + Bi - 2C_{i+1} \dots\dots\dots\dots (2)$$

Thinking about (2), one might imagine of a full adder as a shape whose operation depends on the carry o/p of the $(i+1)$ $n\text{^}th$ bit position $(Ci+1)$ and its entered operand bits. For this structure, the o/ps are the sum and the carry signals with the identical weights.

Based totally on the above dialogue, we advise a family of full adders for the RCPFA shown in Fig. 2. As shown in Fig. 2, those complete adders have 4 i/ps and three o/ps. The i/ps are the enter operands (Ai and Bi), the carry o/p of the subsequent bit position$(Ci+1)$, and a forecast signal (Fi). The RCPFA determines the summation result (Si), carry (Ci), and the forecast signal $(Fi+1)$ as its o/p alerts.

As declared prior to as, the advantage of the RCPA is that the worth of the error is within the trail of decrease among the bit significance. Which implies that the accumulative impact of the error (e.g., because of the delay model) within the route of the carry propagation is decrease for bits with higher significances

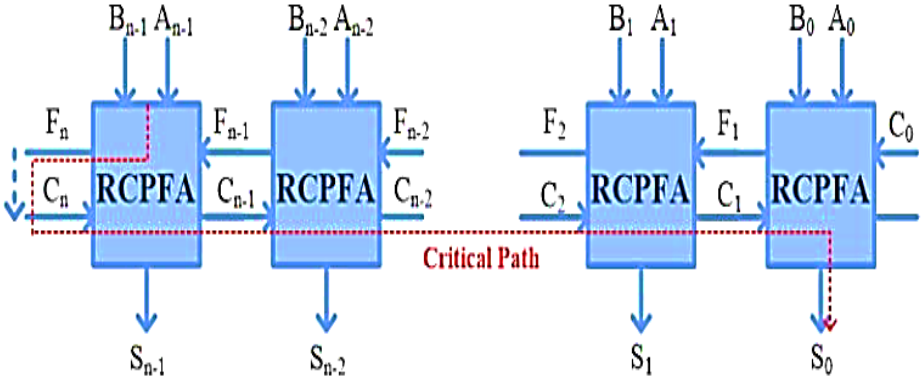


Fig.2 n-bit RCPA.

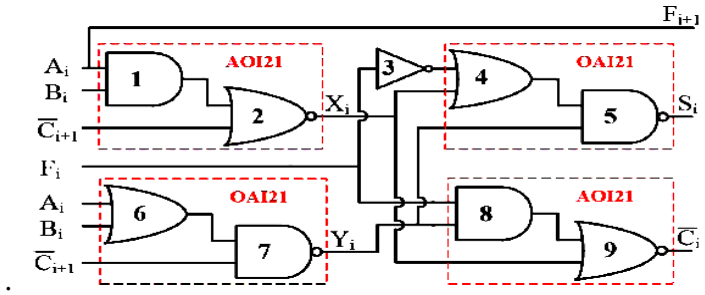
To determine a structure for RCPFA, the Karnaugh maps of the summation end result (Si) and carry (Ci)were drawn based totally on (2) and considering the forecast signal as an i/p (Fig. three) The Boolean contributors of the own family among i/ps for generating Si and Ci are obtained as

$$Si = \underline{C_{i+1}}F_i + \underline{C_{i+1}}Ai + \underline{C_{i+1}}Bi + Ai\,Bi\,Fi \ldots\ldots\ldots (3)$$

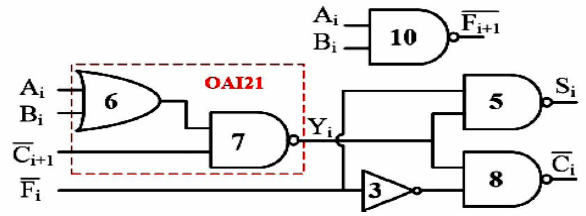
$$Ci = C_{i+1}Fi + C_{i+1}\underline{Ai} + C_{i+1}\underline{Bi} + \underline{Ai\,Bi}Fi \ldots\ldots\ldots (4)$$

Karnaugh maps for signals Si and Ci of the general form of RCPFA.

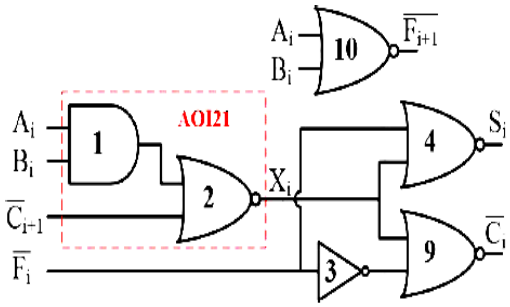
Primarily based on our requirement we design 3 styles of ReverseCarryPropagate adders the designs of those adders are given beneath. by using the use of these proposed adders we will put into effect 3 varieties of reverse propagate adders and are used in the vicinity of approximate adders that is proven on determine 1



(a)



(b)



(c)

Fig.4 Internal structures of the (a) RCPFA-D1,

(b) RCPFA-D2, (c) RCPFA-D3

The architectural representation of an n-bit adder that is designed with the help of a ReverseCarryPropagate adder is shown below.

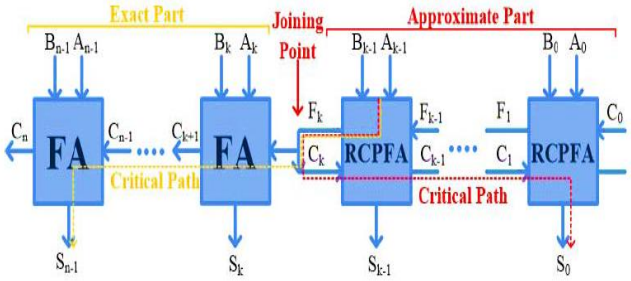


Fig.5 The figure depicts an n-bit adder with RCPA as mentioned earlier. If the carry propagates in the reverse or counter flow manner then the weights of the carry would decrease, this property helps having less vulnerability to the delay version (because of method and supply voltage versions) impact for this adder in comparison to other proposed approximate FAs. This is particularly effective inside the case of hybrid adders with large sizes for the approximate part which determines the crucial route of the adder. The proposed RCPFAs can be used in hybrid adders whose popular n-bit structure based totally at the RCPFAs are depicted in Fig. 8. Obviously, the design parameters of the adder rely on the width of the approximate component.

III. PROPOSED HYBRID ADDER

Here on this paper we advocate a brand new idea that's called as hybrid n-bit adder wherein we have two one-of-a-kind styles of n/2 bit adders are collectively to form an n bit adder. To enhance the general performance in phrases of delay we have a tendency to use a parallel prefix adder referred to as KoggeStone adder. The delay of an adder depends upon on however fast the carry reaches every bit operates. Therefore, the foremost problem within the layout of binary addition is that the carry chain as a result of the dimension of the input quantity will increase the length of the carry chain and delay can boom. To reduce the delay and to boost the performance, the parallel prefix adders will be utilized. The construct in parallel prefix adders is to reason a tiny low establishment of intermediate prefixes so find the large cluster prefixes, until all of the carry bits are calculated. Parallel Prefix addition of the operands A&B of width n is finished in 3 steps as given underneath

1. Pre-Processing
2. Internal Carry Generation
3. Post-Processing

Pre-processing stage:

Here in the 1st level, we shall calculate the (Gi) Generate-signals & (Pi) Propagate-signals, which are used to generate carry i/p of every adder. A&B are i/p's & there alerts are given by the equation one & two.

$$Pi = AiBi \dots\dots (5)$$

$$Gi = Ai.Bi \dots\dots (6)$$

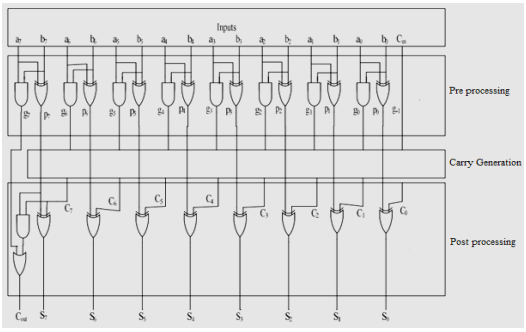


Fig.6 Overall architecture of Parallel prefix addition

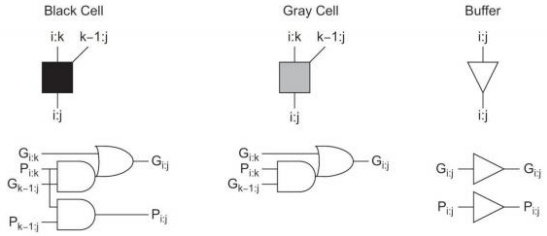
Carry generation stage:

Here in the 2nd level, as we know that we compute Gi & Pi signals and the computation flow is in parallel and it is identical for every bit. After the calculation of an extra bit named carry in parallel they can be divided into smaller portions. Carry operator contains 2 AND gates, 1 OR gate. It makes use of propagate and generate as intermediate indicators which might be given by the equations three & four.

$$P_{(i:k)} = P_{(i:j)} \cdot P_{(j-1:k)} \dots\dots (7)$$

$$G_{(i:k)} = G_{(i:j)} + \left(G_{(j-1:k)} \cdot P_{(i:j)}\right) \dots\dots (8)$$

This carry is generated with the aid of the usage of different cellular structures known as Grey Cell, Black Cell and Buffer Cell. By way of the usage of this cell structures **we are going to** calculate final carry and are identical for all parallel prefix adders however the layout of carry generation is one in every of a sort. Fig.7 Black Cells, Gray Cells and Buffer cell used for carry generation stage



Post Processing:

This is the ultimate level; here the total bits are generated. The total bits are generated each with the helpful resource of using easy XOR gates or via the usage of conditional sum adders. In conditional total adders, for every bit role, tentative sums may be generated and also the best one is perhaps selected while the applicable carry for that bit arrives. KoggeStone prefix adder is one among the fast adder design, because of its very high performance it is used in VLSI implementations. Kogge-Stone adder has large area with minimal fan-out. The KoggeStone adder is extensively known as a parallel prefix adder that performs fast logical addition.

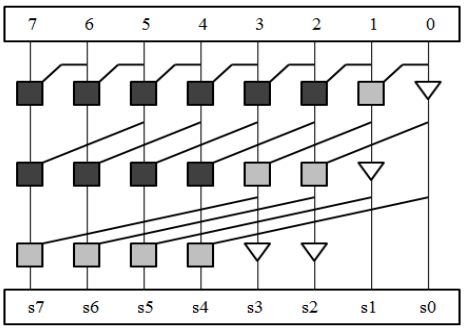


Fig.8 Carry generation of an 8-bit Kogge stone adder

Proposed Adder architecture is shown in below figure

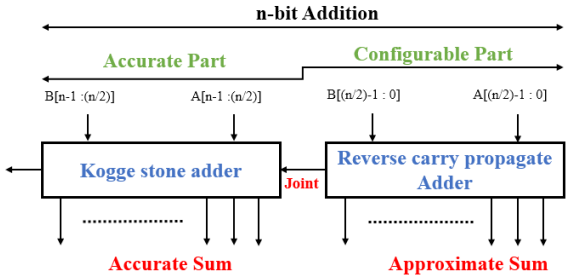


Fig.9 Proposed Hybrid adder architecture

IV. RESULTS AND DISCUSSION

By imposing the adder with two sub adders like Kogge stone adder and Reverse Carry Propagate adder we will have better in terms of delay. Right here on this paper we present 16-bit and 32-bit adders with 3 one of a kind designs of Reverse Carry Propagate adders. The consequences are supplied within the beneath table.

Table 1 Comparison between Existing and proposed Adders

Adder Type	Existing		Proposed	
	Area	**Delay**	**Area**	**Delay**
16bit_d1	45	13.341	62	13.003
16bit_d2	34	13.322	50	10.982
16bit_d3	33	13.308	48	11.296
32bit_d1	95	21.829	148	22.461
32bit_d2	75	21.809	132	15.318
32bit_d3	80	21.765	137	16.296

V. CONCLUSION

In this paper we have designed and carried out an n-bit adder with a hybrid architecture where we use 2 sorts of adders for implementation of large adder. We use approximation in decrease aspect addition this is least vast aspect and correct addition in better side this is most giant aspect. The accurate adder we used on this challenge is a parallel prefix adder referred to as Kogge stone adder and the approximate adder we used is the RCPA we proposed in this paper. With the aid of this architecture we are able to get better delay whilst degrading the accuracy and area.

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