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Low Complexity of VLSI Computational Architectures for the ACT Techniques

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Abstract:-

The discrete cosine transform (DCT) is a widely-used and important signal processing tool employed in a plethora of applications. Typical fast algorithms for nearly-exact computation of DCT require floating point arithmetic, are multiplier intensive, and accumulate round-off errors. Recently proposed fast algorithm arithmetic cosine transform (ACT) calculates the DCT exactly using only additions and integer constant multiplications, with very low area complexity, for null mean input sequences. The ACT can also be computed non-exactly for any input sequence, with low area complexity and low power consumption, utilizing the novel architecture described. However, as a trade-off, the ACT algorithm requires 10 non-uniformly sampled data points to calculate the eight-point DCT. This requirement can easily be satisfied for applications dealing with spatial signals such as image sensors and biomedical sensor arrays, by placing sensor elements in a non-uniform grid. In this work, hardware architecture for the computation of the null mean ACT is proposed, followed by a novel architecture that extend the ACT for non-null mean signals. All circuits are physically implemented and tested using the Xilinx XC6VLX240T FPGA device and synthesized for 45 nm TSMC standard-cell library for performance assessment.

***Keywords**: - Discrete Cosine Transform, Trade-Off, Arithmetic Cosine Transform(ACT), Low Area Complexity and Low Power Consumption.*

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I. Introduction

Over the past several years, the wavelet transform has gained widespread acceptance in signal processing in general and in image compression research in particular. In applications such as still image compression, Discrete Wavelet Transform (DWT) based schemes have outperformed other coding schemes like the ones based on Discrete Cosine Transform (DCT). The DWT has been introduced as a highly efficient and flexible method for sub band decomposition of signals. The two dimensional DWT (2D-DWT) is nowadays established as a key operation in image processing. This is due to the fact that DWT supports features like progressive image transmission (by quality, by resolution), ease of compressed image manipulation, region of interest, etc. In addition to image compression, the DWT has important applications in many areas, such as computer graphics, numerical analysis, radar target distinguishing and so forth. The high algorithmic performance of the 2D DWT in image compression justifies its use as the kernel of both the JPEG2000 still image compression standard and the MPEG-4 texture coding standard. It is widely recognized that the LeGall (5, 3) and the Daubechies (9, 7) filters are among the best filters for DWT-based image compression. In fact, the JPEG2000 image coding standard employs the (5, 3) and the (9, 7) filters as the default wavelet filters for respectively loss and lossy compression. The JPEG2000 can compress images 100 times smaller than the original image.

With this compression ratio, the reconstructed image of the JPEG2000 still provides good visual quality. The coding efficiency of the JPEG2000 comes with the cost. Several years passed by since the JPEG2000 standard was approved in 2002. However, there are not many consumer products that support most features of the JPEG2000 available today. The real-time constraint and cost effectiveness are still major issues for the realization of the JPEG2000 into consumer products. The 2D-DWT is one of the main resources intensive components of JPEG2000; it demands massive computations and represents one of the critical parts in the design and implementation of the JPEG2000 standard. Hence, it requires a parallel and pipelined architecture to perform real-time or on-line video and image coding and decoding, and to implement high-efficiency application-specific integrated circuits (ASIC) or field programmable gate array (FPGA). Up to now, much work has been performed on DWT theory and many VLSI architectures have been proposed. Mallet combined the Wavelet transform and filter bank into a single transformation. Several VLSI architectures have been proposed for computing the 2D-DWT. They are mainly based on convolution scheme and lifting scheme. The lifting scheme can reduce the computational complexity by exploiting the similarities between high and low pass filters and it usually requires fewer multipliers and adders than the convolution scheme. Some architecture for DWT has been proposed to meet the real time requirement in many applications for convolution scheme.

Data compression is the technique to reduce the redundancies in data representation in order to decrease data storage requirements and hence communication costs. Reducing the storage requirement is equivalent to increasing the capacity of the storage medium and hence communication bandwidth. Thus the development of efficient compression techniques will continue to be a design challenge for future communication systems and advanced multimedia applications. The data compression algorithms can be broadly classified in two categories – lossless and lossy. Usually lossless data compression techniques are applied on text data or scientific data. The discrete wavelet transform (DWT) is being increasingly used for image coding. It is due to the fact that DWT supports superior features like progressive image transmission by quality or by resolution. The DWT is the key component of the JPEG2000 system, and it also has been adopted as the transform coder in MPEG-4 still texture coding. However, the DWT requires much more computation than the discrete cosine transform (DCT) because of filter computation. Recently, lifting scheme widely used for DWT leads a speedup and a fewer computation compared to the classical convolution-based method.

Daubechies and Sweldens first derive the lifting-based discrete wavelet transform to reduce complex operations. The lifting-based DWT has several advantages including entire parallel operations, “in place” computations of the DWT, integer-to-integer transform, symmetric forward and inverse transform, etc. Hence, the lifting scheme is deservedly adopted in the JPEG 2000 image standard. Several efficient DWT architectures are presented by using the lifting-scheme. In general, 2- D DWT is realized by directly executing the 1-D DWT row by row and then column by column. However, the huge frame memory is required to store the intermediate coefficients. Due to the N2 size of the frame memory, it is usually devised to be the external memory of the DWT chip. Thus, the high external memory bandwidth leads to great power consumption in the 2-D DWT architecture.

The line-based architecture proposed is an alternative method to eliminate the frame memory by performing 1-D DWT in both directories simultaneously. In order to reduce the external memory access, the line-based method

requires some internal line buffer to store the intermediate coefficients. Tseng et al. focus their idea on optimizing the internal line buffer size for the line based 2-D DWT architectures. Moreover, several line-based architectures are proposed based on the factorized lifting scheme. It present a lifting-based forward and inverse DWT architecture with a general 1-D DWT core to support various DWT filters in JPEG 2000. A systematic method with systolic array mapping is proposed to construct several efficient architectures for 1-D and 2-D lifting-based DW. Liao et al. propose two DWT architectures with recursive and dual scan methods for multi-level and single level 2-D DWT decomposition, respectively.

II. EXISTING SYSTEM

2.1 DWT

DWT analyzes the data at different frequencies with different time resolutions. Fig shows the DWT decomposition of the image. The DWT decomposition involves low-pass „l" and high pass „h" filtering of the images in both horizontal and vertical directions. After each filtering, the output is down-sampled by two. Further decomposition is done by applying the above process to the LL sub-band.

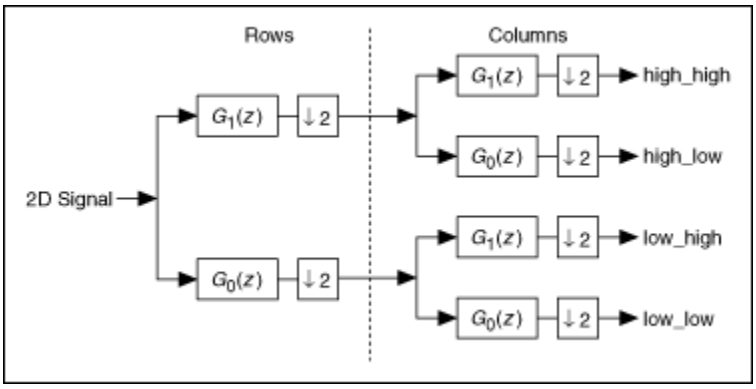

Fig 1: DWT decomposition of the image

Wavelets convert the image into a series of wavelets that can be stored more efficiently than pixel blocks. Wavelets have rough edges, they are able to render pictures better by eliminating the ―blockiness‖. In DWT, a timescale representation of the digital signal is obtained using digital filtering techniques. The signal to be analyzed is passed through filters with different cut-off frequencies at different scales. It is easy to implement and reduces the computation time and resources required. A 2-D DWT can be seen as a 1-D wavelet scheme which transform along the rows and then a 1-D wavelet transform along the columns, The 2-D DWT operates in a straight forward manner by inserting array transposition between the two 1-D DWT. The rows of the array are processed first with only one level of decomposition. This essentially divides the array into two vertical halves, with the first half storing the average coefficients, while the second vertical half stores the detail coefficients.

2.2 Arithmetic in lifting DWT

The lifting scheme provides many advantages, such as fewer arithmetic operations, in place implementation and easy management of boundary extension compared to convolution based DWT architectures. For simplicity, we use the popular bi-orthogonal wavelet (5,3) filter, adopted in JPEG 2000, in order to explain the redundancy in the arithmetic operation involved in the calculation of the lifting-based DWT computation.

The convolution-based 1-D DWT requires both a large number of arithmetic computations and a large memory for storage. Such features are not desirable for either high speed or low-power image processing applications. Recently, a new mathematical formulation for wavelet transformation has been proposed as a light-weighted computation method for performing wavelet transform. The main feature of the lifting-based wavelet transform is to break-up the high pass and the low pass wavelet filters into a sequence of smaller filters. The lifting scheme requires fewer computations compared to the convolution-based DWT. Therefore the computational complexity is reduced to almost a half of those needed with a convolution approach. As a result, lifting has been suggested for implementation of DWT in JPEG2000 standard.

The basic idea of lifting scheme is first to compute a trivial wavelet (or lazy wavelet transform) by splitting the original 1-D signal into odd and even indexed subsequences, and then modifying these values using alternating prediction and updating steps. The lifting scheme algorithm can be described as follow: -

Split step: The original signal, X(n), is split into odd and even samples (lazy wavelet transform).

Lifting step: This step is executed as N sub-steps (depending on the type of the filter), where the odd and even samples are filtered by the prediction and update filters, Pn(n) and Un(n).

Normalization or Scaling step: After N lifting steps, a scaling coefficients K and 1/K are applied respectively to the odd and even samples in order to obtain the low pass band (YL(i)), and the high-pass sub-band (YH(i)). Fig illustrates how the lifting scheme can be implemented using these steps. The diagram shows the lifting scheme for Daubechies (9, 7) bi-orthogonal filter adopted in JPEG2000 standard for lossy compression.

III. PROPOSED SYSTEM

Discrete cosine transform (DCT) is widely used in multimedia communications such as image and video which require high volume of data transmission. An 8x8 2-D discrete cosine transform is used in image and video compression standards. DCT is a computation intensive operation. It requires a large number of adders and multipliers for direct implementation. Multipliers consume more power and hence distributed arithmetic (DA) is used to implement multiplication without multiplier so, DA acts as a multiplier. In the proposed method, VLSI architecture of 1-D DCT based distributed arithmetic (DA) is for low hardware circuit cost as well as low power consumption. The proposed 1-D DCT architecture is implemented in Xilinx ISE Simulator. With proposed 1-D DCT architecture, 2-D DCT will implement using row column decomposition technique. Results of proposed architecture with existed architecture are compared and delay and power is reduced to 50%. Further, this project can be extendable by using any other type of faster adder/multiplier in terms of area, speed and power.

The discrete cosine transform (DCT) is a widely-used and important signal processing tool employed in a plethora of applications. Typical fast algorithms for nearly-exact computation of DCT require floating point arithmetic, are multiplier intensive, and accumulate round-off errors. Recently proposed fast algorithm arithmetic cosine transform (ACT) calculates the DCT exactly using only additions and integer constant multiplications, with very low area complexity, for null mean input sequences. The ACT can also be computed non-exactly for any input sequence, with low area complexity and low power consumption, utilizing the novel architecture described. However, as a trade-off, the ACT algorithm requires 10 non-uniformly sampled data points to calculate the eight-point DCT. This requirement can easily be satisfied for applications dealing with spatial signals such as image sensors and biomedical sensor arrays, by placing sensor elements in a non-uniform grid. In this work, a hardware architecture for the computation of the null mean ACT is proposed, followed by a novel architectures that extend the ACT for non-null mean signals. All circuits are physically implemented and tested using the Xilinx XC6VLX240T FPGA device and synthesized for 45 nm TSMC standard-cell library for performance assessment.

The proposed DWT architecture consists of predict module, update module, and address generation module, control unit and a set of registers to establish data communication between the modules. This architecture can be used to carry out both forward and inverse discrete wavelet transform.

IV. PROPOSED SYSTEM DESCRIPTION

The predict module for (5, 3) wavelet. Initially, the input register R1 is loaded with the even sample from the input RAM. In the meantime, they predict filter coefficient „α" and the corresponding odd sample are made available to calculate the detailed coefficient dj-1,i. The second register R2 stores the output of the multiplier in the current cycle and in the meantime the register R2 supplies the multiplier output obtained in the previous cycle. Thus, we reduce the number of multipliers required for predict operation for (5,3) wavelet to one whereas the number required for the architecture described] is two. For (5,3) wavelet, we can use shifters instead of multipliers.

Discrete cosine transform (DCT) is unitary of the major compression schemes owing to its near optimal performance and delivers energy compaction efficiency greater than any other transform. The transformation algorithm is presented.

4.1 DCT Architecture

By using DCT architecture, then DWT is that there is higher throughput, lesser complexity and also no need to manipulate complex number. When computing 2D DCT, a greater number of multipliers and adders are required for enforcing the compression organization in harder, which shows the most time consuming process, it can

be completely avoided in the proposed DA-based DCT architecture with Kogge_Stone_Adder. A minimum number of additions are used to the DCT based on the Distributed Arithmetic.

A discrete cosine transform (DCT) expresses a finite sequence of data points in terms of a sum of cosine functions oscillating at different frequencies. DCTs are important to numerous applications in science and engineering, from lossy compression of audio (e.g. MP3) and images (e.g. JPEG) (where small high-frequency components can be discarded), to spectral methods for the numerical solution of partial differential equations. The use of cosine rather than sine functions is critical for compression, since it turns out (as described below) that fewer cosine functions are needed to approximate a typical signal, whereas for differential equations the cosines express a particular choice of boundary conditions.

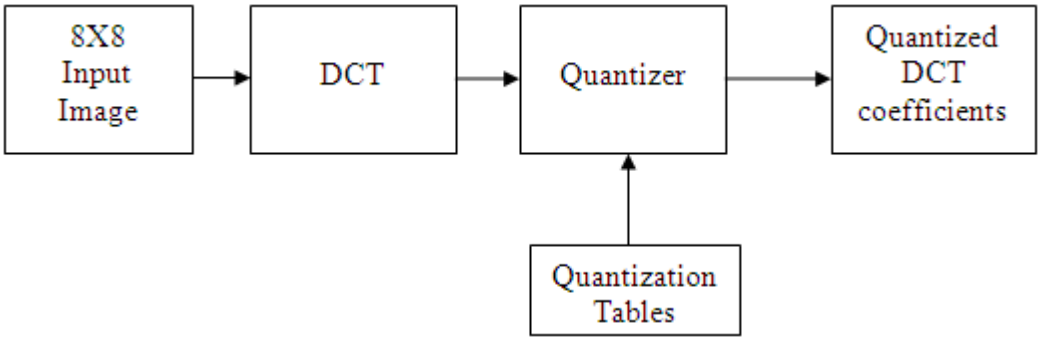

Fig 2: DCT Architecture

In particular, a DCT is a Fourier-related transform similar to the discrete Fourier transform (DFT), but using only real numbers. DCTs are equivalent to DFTs of roughly twice the length, operating on real data with even symmetry (since the Fourier transform of a real and even function is real and even), where in some variants the input and/or output data are shifted by half a sample. There are eight standard DCT variants, of which four are common.

The most common variant of discrete cosine transform is the type-II DCT, which is often called simply "the DCT". Its inverse, the type-III DCT, is correspondingly often called simply "the inverse DCT" or "the IDCT".

There has been a lot of research both in industry and academia on how to efficeintly implement a fast DCT/IDCT hardware algorithm. Dae Won Kiln, et. al [1], proposed and implemented a hardware Distributed Arithmetic(DA) method with radix-2 multibit coding with minimum resource requirement by using transpose memory. Atitallah et. al [2] compared Loeffler and DA algorithms to implement compression in H.264 nad MPEG. Martuza et. al [3] presented a hybrid architecture for IDCT computation based on the symmetric structure of matrices and similarity in matrix operations. The proposed architecture derives its inspiration from all the above well set examples

A discrete cosine transform (DCT) expresses a sequence of finitely many data points in terms of a sum of cosine functions oscillating at different frequencies i.e. it transforms a signal from a spatial representation into a frequency representation. In an image, most of the energy will be concentrated in the lower frequencies, so if I transform an image into its frequency components and discard the higher frequency coefficients, I can reduce the amount of data needed to describe the image without sacrificing too much image quality. This is why DCT is popularly used in several image compression algorithms. The DCT function used in image processing consists of sum of weighted cosine functions at different frequencies.

The Discrete Cosine Transform is one of the most widely transform techniques in digital signal processing. In addition, this is also most computationally intensive transforms which require many multiplications and additions. Real time data processing necessitates the use of special purpose hardware which involves hardware efficiency as well as high throughput. Many DCT algorithms were proposed in order to achieve high speed DCT. Those architectures which involves multipliers ,for example Chen's algorithm has less regular architecture due to complex routing and requires large silicon area. On the other hand, the DCT architecture based on distributed arithmetic (DA) which is also a multiplier less architecture has the inherent disadvantage of less throughputs because of the ROM access time and the need of accumulator. Also this DA algorithm requires large silicon area if it requires large ROM size. Systolic array architecture for the real-time DCT computation may have the large number of gates and clock skew problem. The other ways of implementation of DCT which involves in multiplierless, thus power efficient and

which results in regular architecture and less complicated routing, consequently less area, simultaneously lead to high throughput. So for that purpose CORDIC seems to be a best solution.

CORDIC offers a unified iterative formulation to efficiently evaluate the rotation operation. This thesis presents the implementation of 2D Discrete Cosine Transform (DCT) using the Angle Recoded (AR) Cordic algorithm, the new scaling less CORDIC algorithm and the conventional Chen's algorithm which is multiplier dependant algorithm. The 2D DCT is implemented by exploiting the Separability property of 2D Discrete Cosine Transform. Here first one dimensional DCT is designed first and later a transpose buffer which consists of 64 memory elements, fully pipelined is designed.

4.2 Design flow

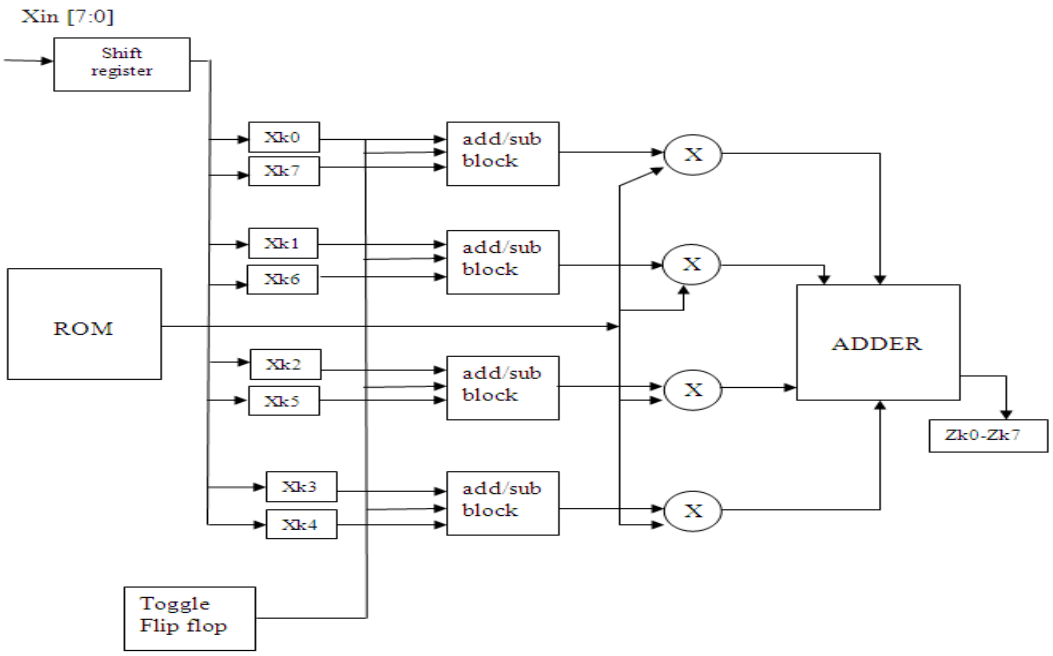

Fig 3: Design Flow of DCT

The design flow of a system constitutes various levels of abstraction. When a system is designed with an emphasis on power optimization as a performance goal, then the design must embody optimization at all levels of the design. In general there are three main levels on which energy reduction can be incorporated. The system level, the logic level, and the technological level. For example, at the system level power management can be used to turn off inactive modules to save power, and parallel hardware may be used to reduce global interconnect and allow a reduction in supply voltage without degrading system throughput. At the logic level asynchronous design techniques can be used. At the technological level several optimizations can be applied to chip layout, packaging and voltage reduction. Low power design problems are broadly classified in to

1. Analysis
2. Optimization

Analysis: These problems are concerned about the accurate estimation of the power or energy dissipation at different phases of the design process. The purpose is to increase confidence of the design with the assurance that the power consumption specifications are not violated. Evidently, analysis techniques differ in their accuracy and efficiency. Accuracy depends on the availability of design information. In early design phases emphasis is to obtain power dissipation estimates rapidly with very little available information on the design. As the design proceeds to reveal lower-level details, a more accurate analysis can be performed. Analysis techniques also serve as the foundation for design optimization.

Optimization: Optimization is the process of generating the best design, given an optimization goal, without violating design specifications; an automatic design optimization algorithm requires a fast analysis engine to evaluate the merits of the design choices. A decision to apply a particular low power design technique often involves tradeoffs from different sources pulling in various directions. Major criteria to be considered are the impact on circuit delays, which directly translates to manufacturing costs. Other factors of chip design such as design cycle

time, testability, quality, reliability, reusability; risk etc may all be affected by a particular design decision to achieve the low power requirement. The task of a design engineer is to carefully weigh each design choice with in specification constraints and select the best implementation. Before we set to analyze or optimize the power dissipation of a VLSI chip, the basic understanding of the fundamental circuit theory of power dissipation is imminent. Further is the summary of the basic power dissipation modes of a digital chip.

V. SIMULATION & SYNTHESYS RESULTS

5.1 RTL Synthesis Result

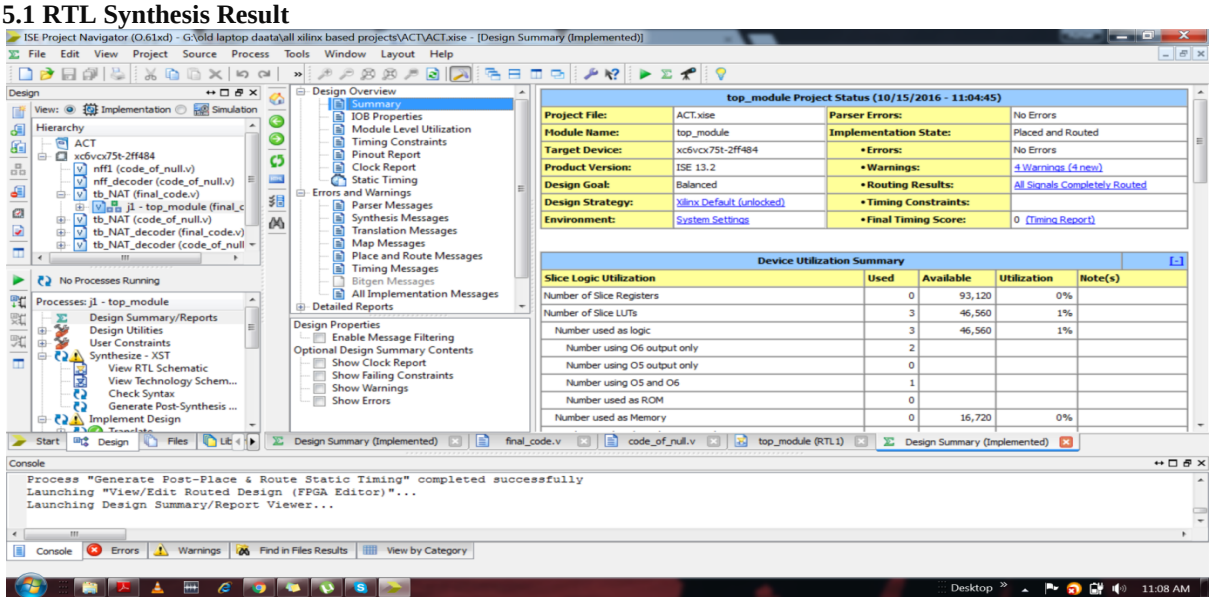

Fig 4: Design Summary Data

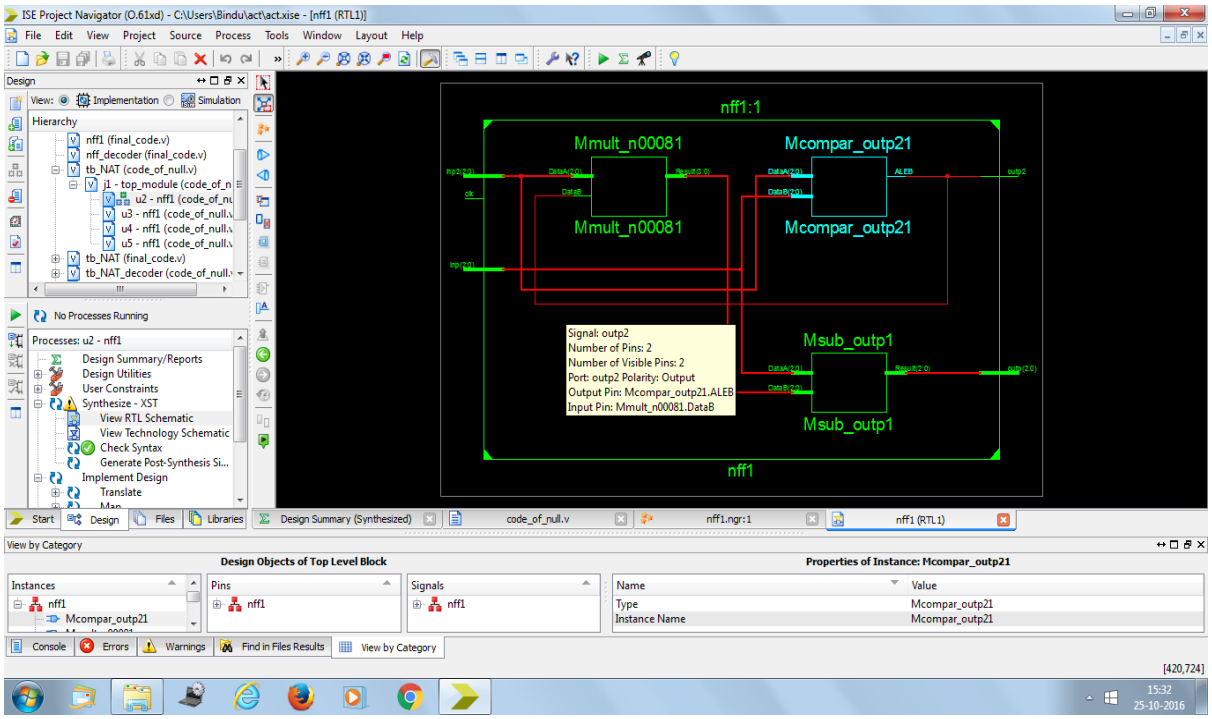

Fig 5: RTL Synthesis Result 1

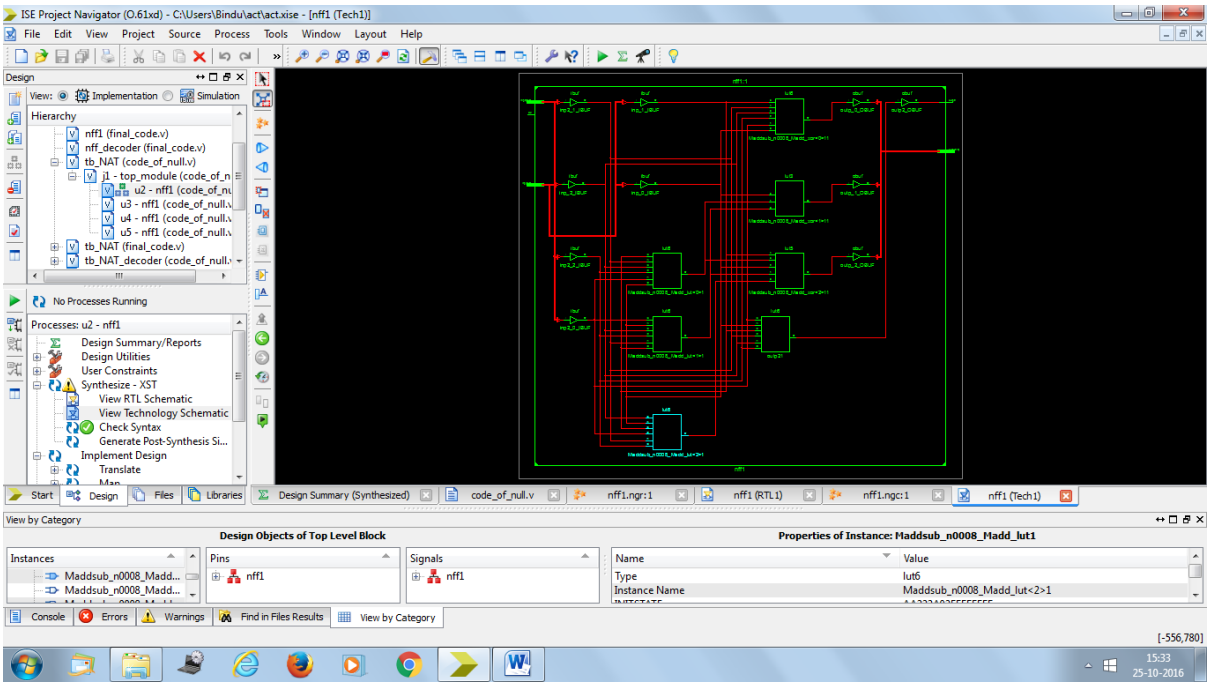

Fig 6: RTL Synthesis Result 2

5.2 Simulation Result

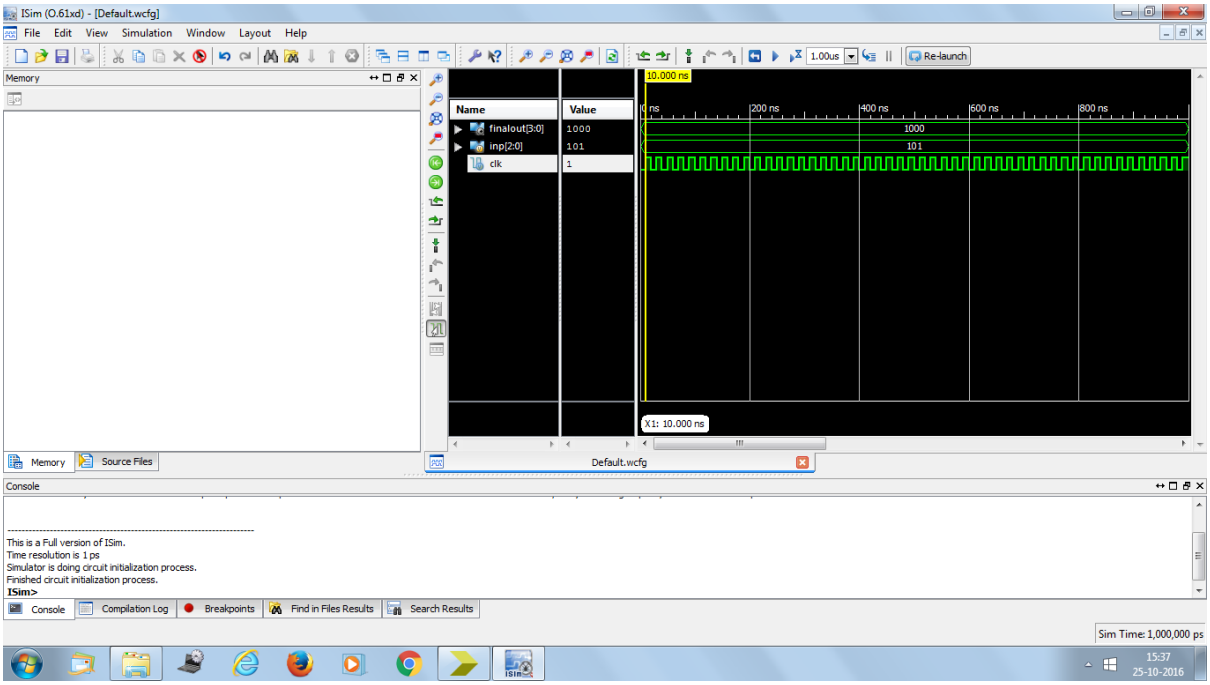

Fig 7: RTL Simulation Result 1

Advantages

1. Low power consumption, occupies less area.
2. Speed of operation is high.

Applications

1. This technique is used in image and video applications.
2. It is used in Digital signal processing and Digital image technologies.
3. These techniques are used in Image compression.

VI. CONCLUSION & FUTURE SCOPE

The 2D-DCT combined with Forward and Inverse is designed using VHDL. This has proposed a architecture based on the row column decomposition for computation of 2D-DCT. Parallel process causes latency in the system. Latency produced from this system is 113 clock cycles for 2D-DCT and 112 for 2D-IDCT. As we implement in this project by 8×8 block, in future we may implement it by 16×16, 32×32 up to a standard size of the image. The row column decomposition method reduces the hardware complexity as per the other methods. As the block of the size increases hardware also increases but we can implement it easily by this row column decomposition method.

In this project we proposed 1 D, 2 D discrete cosine transform architecture using Verilog, In future we will implement this in terms of less complexity, for this technique power consumption is very less, and also we will increase of point DCT, in this complex multiplications are present, so in future we will introduce advanced multipliers.

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