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Static Random Access Memory with Half V_{dd} and Dynamically Powered Read Port for High Speed and Low Switching Power Capabilities

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***Abstract*- In this paper, we introduce a 10-transistor static random access memory cell that features an unbalanced read decoupled bit line (RBL) with a 4T read pin for high-speed operation. Based on the stored data bit, the RBL is pre-charged to half the cell's supply voltage and allowed to charge and discharge. The Complementary Data (QB) node is driven by an inverter that connects the RBL to the virtual power rails via a transmission gate during read operation. RBL rises to VDD level for a read of 1 and dumps to ground level for a read of 0. During write mode and standby mode, the virtual power rails have the same RBL precharge level value. During the reading process, these are connected to actual supply levels. Dynamic control of virtual rails significantly reduces RBL leakage. The proposed 12T cell is larger compared to the SRAM 10T and reduces read lag by more than 50% compared to the 10T. The general performance characteristics of the 12T and 10T are similar, and the general designs are designed and implemented at Tanner EDA.**

***Keywords*— 10T, charge recycling, leakage reduction, low power, precharging , single ended (SE) read bit line (RBL), static random access memory (SRAM), virtual rails.**

I. INTRODUCTION

SRAM (static RAM) is random access memory (RAM) that retains bits of data in its memory as long as power is applied. Unlike dynamic RAM (DRAM), which stores bits in cells made up of a capacitor and a transistor, SRAM does not need to be updated periodically. Static RAM provides faster data access and is more expensive than DRAM. SRAM is used for a computer's cache memory and as part of the random access memory digital-to-analog converter on a video card.

MOSFET MEMORY CONCEPT

The emergence of the MOSFET-based memory concept was first commercialized and refined in the 1970s. In 1968, IBM's Robert Dennard proposed the dynamic memory cell with a single MOSFET and capacitor. The first 2k-bit MOSFET-based dynamic random access memory (DRAM) chip was developed in 1971 with several process improvements in leakage control. However, DRAM performance did not keep up with the performance of early processors due to long access times and a higher need for performance. The dynamic nature of DRAM requires that the memory be refreshed periodically so as not to lose the contents of the memory cells.

II. SRAMS AND SOC

SRAMs continue to be important components in a variety of microelectronics applications, from consumer electronics to high-performance computing devices, multimedia, and system-on-chip (SoC) applications. Today's advanced processors and SoC applications require on-chip memory to meet the demands and requirements. However, due to geographical limitations and the high cost of each bit, it is not possible to install the required amount of memory on the chip. A SRAM cache is a group of bistable memory cells with peripheral circuits such as B. Decoders (row and column decoders), logic amplifiers, write drivers and bit line pre-processor circuits , and so on. The six-transistor (6T) SRAM cell is the most widely used standard in the industry; it has its limits. The 6T SRAM not only resists read and write requirements, but also reduces the static read noise margin (RSNM). The main factors to consider when designing SRAM in new nano meter technologies: 1) read stability; 2) written record; 3) reduced internet access; 4) power outage; 5) leakage currents; 6) bitline (BL) ION to IOFF ratio; and 7) diversity. Melting has become a constant in design because we are limited in use and search for low-power circuits, designs and system-level technologies. In addition, the static random access memory (SRAM) is the most important digital macro and its share in a system-on-chip (Soc) is constantly increasing.

Melting has become a major design influence [1], [2] as we hit the usability limit and circuit, design and system level techniques with low power consumption are explored [3], [4].

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In addition, static random access memory (SRAM) is the most important digital macro device and its share in a system-on-chip (Soc) is constantly increasing as seen in innovations in leakage power related topics [5]. Reducing the power of the SRAM will not only reduce the power of the entire system, but will increase the yield and increase the reliability of the Soc. Although the six transistor (6T) SRAM cell is the most widely used standard in the industry, it has its own limitations. The 6T SRAM not only resists read and write requirements, but also reduces the static read noise margin (RSNM).

III. EXISTING METHOD

An SRAM cell must hold, read and write data. A SRAM cell uses the concept of cross-coupled inverters (INVs) to store one bit of information in an integrated manner. Input transistors provide the mechanism for read and write operations. Before each input, the column BL pair (BL and BLB) is pre-applied to the supply voltage. For a write operation, one of the previously loaded BLs is released by the write driver. Figure 1(a) shows a single column of M 6T SRAM cells where a cell is in read mode with data = 0 (Qa = 0) while the other M-1 cells are in hold mode. Leakage units are labeled and since all leakage is worst M-1 data store=1 (Qu=1). Iread flows from BL to VSS through AL and NL of the input cell and the BL voltage is reduced. A cell in the BL that does not appear to have BL leakage. IuLeak0 is the main BL leak and IuLeak1 is insignificant because the VDS of AR of the unaccessed cell is large and the VDS of its AL is very small (different from 0 to _VBL). These leakage currents reduce the BL voltage differential development. In the worst case, even if there are many cells in a single column, the leakage BL can lower the voltage BLB which can lead to wrong charging. Therefore, Iread is greater than (M − 1) × IuLeak0, where M is the number of cells in a single column. During reading, the internal node of cell 6T, which stores a zero (Qa), is in the read current path and the voltage increases during the reading process. This voltage increase (_V) affects the measurement of the transistor. For better readings, the β ratio, defined as (((W/L)N)/((W/L)A)) should be greater than 1 (typically 2 to 3). The HSNM and RSNM butterfly curves (top) [24] and the local disturbance of the QB node for a slowly increasing WL signal (bottom) also exist. Increasing the voltage at node Qa not only reduces the cell stability but also helps the overall system.

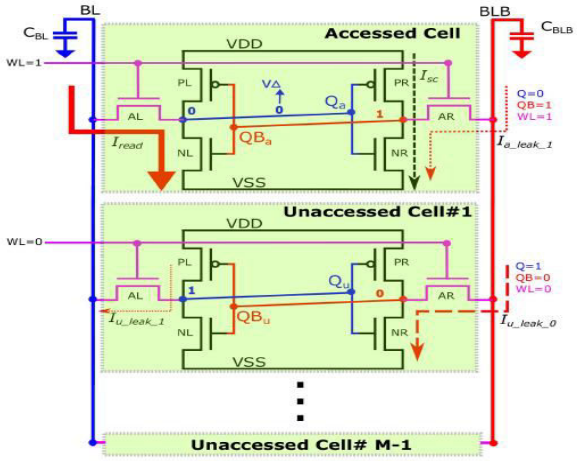

Fig 1: Conventional SRAM Design

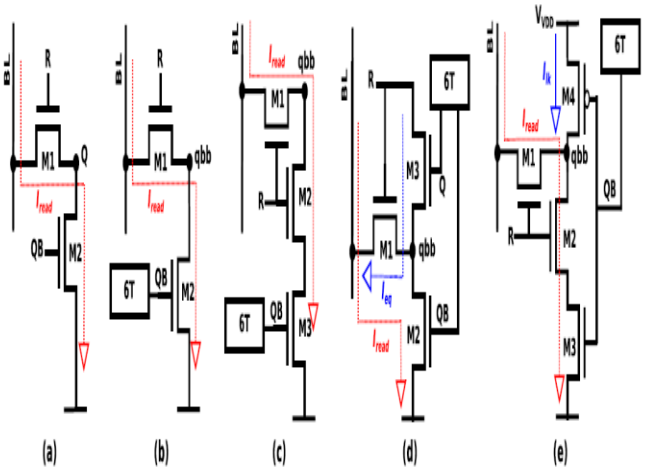

Fig 2: Various SRAM Read ports

IV. PROPOSED METHOD

A 10T SRAM cell with SE RBL is shown in Fig.3. We add a 4T read port to the 6T cell to separate local nodes during the read. The read port consists of an INV P1-N1 driven by the QB node and a transmit gate (TG) P2-N2. The output (Z) of the INV connected via TG to RBL during reading, controlled by (reading) control signals. Also, the read port is used by the virtual control channels, VVDD and VVSS, which are controlled. These virtual control channels (control signals) run and only receive real traffic values during the reading process. To reduce RBL leakage, the level of both electric motors is equal to the RBL precharge level. A 10T SRAM cell using an INV and a TG was previously proposed. However, our proposed 10T plan differs from the previous plan in the following ways. 1) The 10T cell-based INV + TG is application specific while our proposed strategy is generic. 2)

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We have used strong power cables for the read port. 3) We precharge RBL at VDD/2, whereas the previous 10T design eliminated the precharge phase and used INV to fully charge or discharge the RBL.

4) The basic reading technique of both layouts is completely different. The main idea of the proposed design is to "load or unload the VDD/2 read BL for each read". The above design download from VDD to VSS or upload from VSS to VDD.

5) A powerful INV was previously used to create a full VDD swing on the RBL. In the proposed design, RBL is precharged to VDD/2 and only a small voltage differential (comparable to 6T) is created for each read cycle.

6) In the proposed design, the RBL shows some change (positive or negative) from its preloaded value of vdd/2 for each read cycle. However, in the RBL would not change for consecutive similar bit reads. RBL would only change if the consecutive bits read are different.

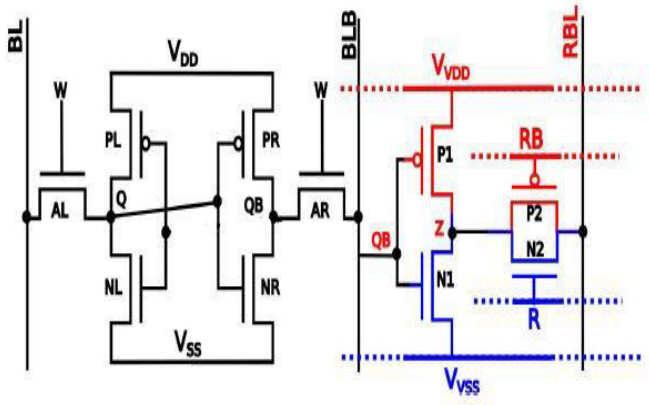

Fig 3: Proposed SRAM cell with row-wise read port dynamic power lines.

V. RESULTS

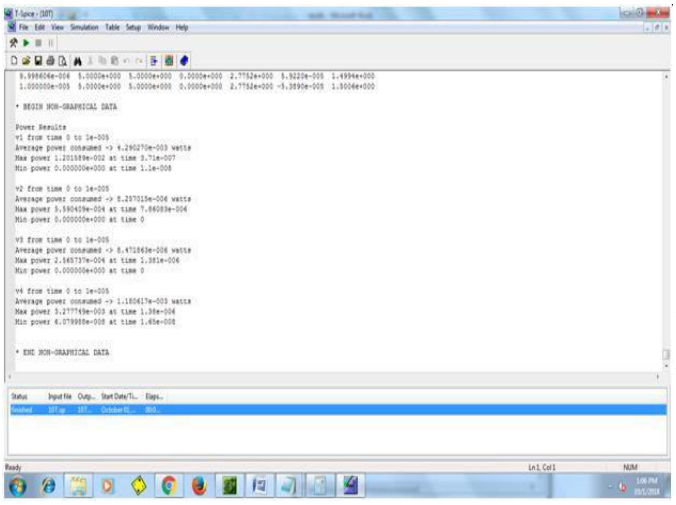

Fig. 4 : Power results for v_1 v_2 and v_3

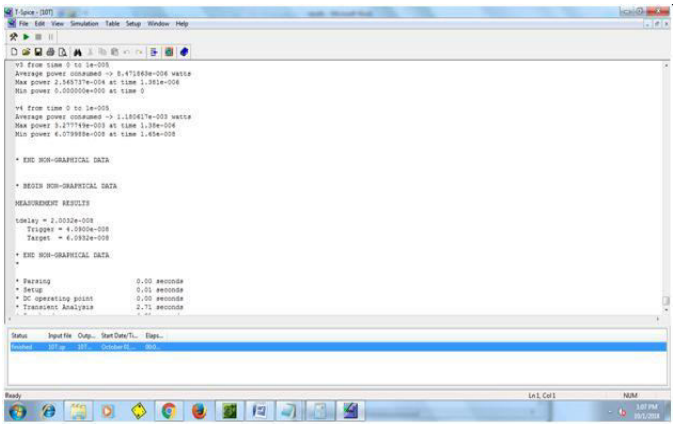

Fig. 5 : Average Power results

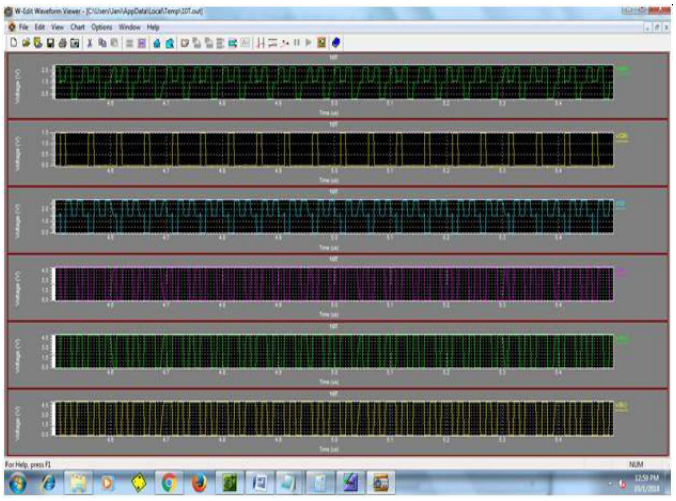

Fig. 6: Graphical representation

VI. CONCLUSIONS

In this document, we introduce our 10T SRAM cell, which uses a 4T read port and SE-RBL. RBL is precharged at half the supply voltage and charges or discharges depending on the bit stored during the read operation. For a read 0 operation, RBL is discharged via TG and the nMOS transistor, and for the next precharge, RBL receives power from VP. For a Read 1 operation, RBL is charged from vdd/2 to vdd through the virtual read port. For the next precharge, the RBL level is

reduced and current flows from RBL to VP. By precharging per VP (which is half of vdd) and charging recycling mechanism, the LP10T only consumes less than the existing system.

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