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An Efficient Novel Approach Paradigm of Single Cycle Switching Access Structure to Eliminate the Peak Power Consumption Problem

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Abstract:

Now a day's the Conventional shift-based scan chains have the drawback of peak power consumption which is reduced by the proposed single cycle access test structure for logic test. With the Most efficient reduction of this power consumption the activity during shift and capture cycles have been achieved. In addition, more accurate circuit behavior can be achieved even at stuck-at and at-speed tests using the proposed methodology. Thereby it accomplishes close proximity to the functional mode during higher frequency operation tests.By using the proposed design minimum number of test cycles can be gained to the existed literature. It is observed that test cycles per net is below 1 for larger designs when tested for simple test pattern generator algorithm without test pattern compression. Has the advantage of independent of the design size and also provides an additional on-chip debugging signal visibility for each register. It is backward compatible to the standard full scan designs and with a minor enhancement existing test pattern generators and simulators can be used and also discussed for the solution of adding built-in self test (BIST) and massive parallel scan chains with the proposed design.The design and implementation of single cycle access test structure for logic test is functionally verified using Xilinx ISE simulator 13.1 and the generated bit stream file is implemented in Spartan 3E XC3S50OE FPGA board, which demonstrates the all-possible combinations of proposed single cycle access test structure for logic test on its LCD display. The pre layout and post layout synthesis and its physical design are performed using cadence RTL Compiler and SOC Encounter tools respectively, with the optimized area, power, and delay.

Key words: Built-in self test (BIST), LCD, RTL Compiler, SOC

INTRODUCTION:

The standard shift scan (SS) method is the most popular test putting into use within the last at least 20 years. Automatic test pattern generation (ATPG) for one after the other VLSI circuits is an NP-complete problem with an increasing more and more as time goes on) complex difficulty. The complex difficulty of combinatorial logic differschanges. Less complex logic is tested within a few act of being taken or controlled by force cycles, creating a huge number of don't cares during the rest of the test, even when test (press or force into a smaller space)ion methods are used. Complex and hard to test logic needs to be stimulated and taken by force quite often but the pattern need to be movedchanged throughout the complete scan chain. One approach to reduce test time is to use parallel scan chain. This leads to a huge increase of parallel scan chains to reduce the length of the scan chains. In order to further reduce test data volume, a built-in-self-test (BIST) machineis used. One approach to

reduce test time is to use parallel scan chain. This leads to a huge increase of parallel scan chains to reduce the length of the scan chains. In order to further reduce test data volume, a built-in-self-test (BIST) machine is used. This project presents a novel scan cell register for logic tests combined with a novel scan cell routing related to the beautiful design and construction of buildings, etc. The structure allows a single cycle access (SCA) to individual register sets. This access big layout plan is basically different to SS. It can be compared to a memory with single cycle two or more things happening at the same time write and not happening at the same time read ability to do things, whereas the remaining memory content registers does not change. The proposed structure is related for pattern driven tests and for BIST. The project provides reasonable data but is not limited to a frozen solution. It also discusses different trade-offs of different other choices. Logic test is a wide field and different users have different preferences. A reference example based on 992 registers is used and should guide through the project.

OBJECTIVE:

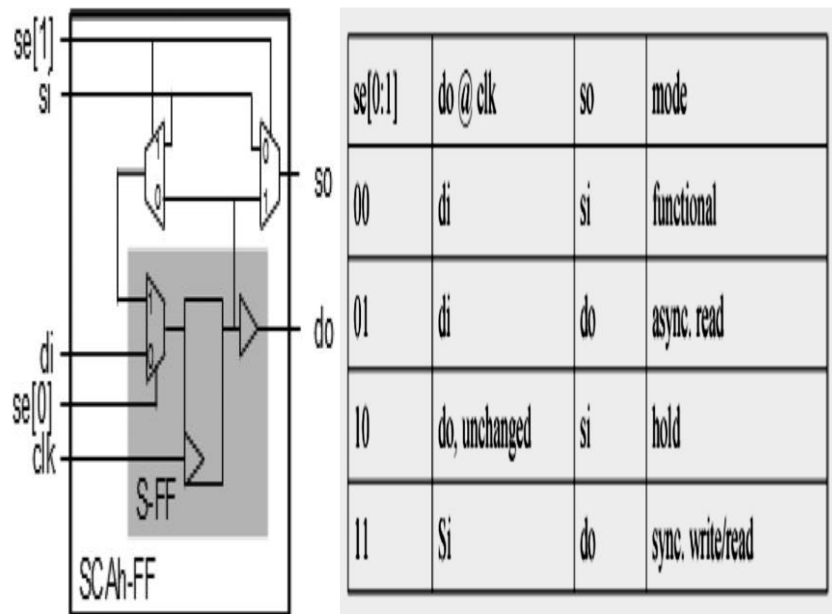
This access big plan plan is basically different to SS (Shift Scan). It can be compared to a memory with single cycle two or more things happening at the same time write and not happening at the same time read ability to do things, whereas the remaining memory content registers does not change. Unlike with a certain number of shift cycles in shift-scan designs, the values can be read and written within one single cycle. This allows higher test frequencies and leads to more realistic test conditions closer to the functional chip behavior during stuck-at and at-speed tests. The proposed structure is related for pattern driven tests and for BIST. The project provides reasonable data but is not limited to a frozen solution.

PROBLEM STATEMENT:

Reduction in average and peak power during test application is important to improve electrical storage device lifetime in portable electronic devices employing occasional self-test and to improve reliabilitycost of testing. This project proposes a having different things working together as one unit solution for peak and average power reduction in test-per-scan BIST by targeting power reduction in both combinational block and scan chain. First, we present a novel circuit way of doing things, called First Level Supply gating (FLS), to almost eliminate power disappearing (or wasting) in combinational logic by hiding signal change (from one thing to another) at the logic inputs during scan shifting. We understandreal the hiding effect by inserting an extra supply gating transistor in the VDD to GND path for the first level gates at the output of scan flip-flops.The most drawback of existing problem is more peak power consumption and more shift and capture cycles. The proposed FLS gating way of doing things makes something as small as possibletreats something important as unimportant power in the combinational block. It not only eliminates unnecessary switching activity in the combinational block, but also provides leakage minimization through application of the best input vector during scan shifting. The proposed scan separating (with a wall) way of doing things reduces average and peak power in the scan chain by (making something as small as possibletreating something important as unimportant) rippling of scan values pre-decidedly.

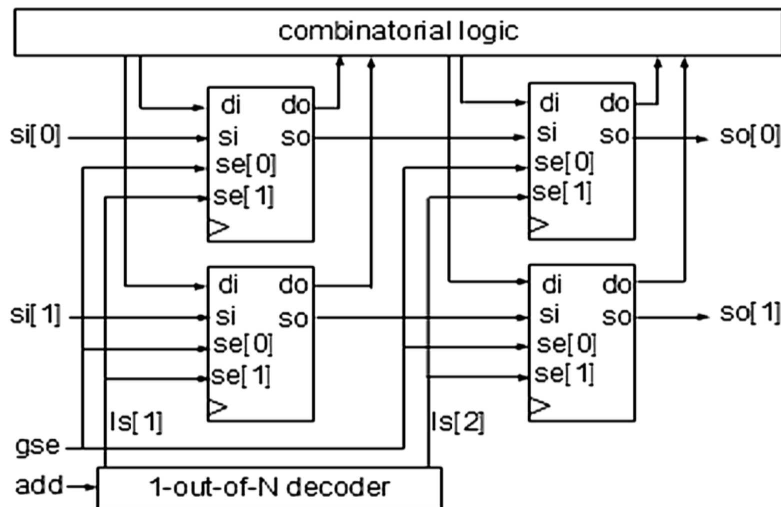
PROPOSED METHODOLOGY:

This research proposes a new single cycle access test structure for logic test. It eliminates the peak power use problem of ordinary shift-based scan chains and reduces the activity during shift and take by forcetake control of cycles. This leads to more realistic circuit behavior during stuck at and at-speed tests. It enables the complete test to run at much higher frequencies equal or close to the one in functional mode. It will be shown, that a lesser number of test cycles can be (accomplished or gained with effort) compared to other published solutions. The test cycle per net based on a simple test pattern generator set of computer instructions without test pattern (press or force into a smaller space) ion is below 1 for larger designs and is independent of the design size. Results are compared to other published solutions on ISCAS'89 net lists. The structure allows an added on-chip (finding and correcting mistakes in) signal visibility for each register. The method is backward compatible to full scan designs and existing test pattern generators and machines (that reproduce the real thing) can be used with a minor improvement. It is shown how to combine the proposed solution with built-in self test (BIST) and huge parallel scan chains.



se[0:1]	do @ clk	so	mode
00	di	si	functional
01	di	do	async. read
10	do, unchanged	si	hold
11	Si	do	sync. write/read

SCAh-FF based on an S-FF.TRUTH TABLE OF SCAh-FF SCAhS connectivity.



Xilinx ISE IMPLEMENTATION:

FDC:C->Q 5 0.626 0.842 SFF2/scanFF/SF1/Q (SFF2/scanFF/SF1/Q)

LUT4:I2->O 1 0.479 0.000 Combinationallogic/Mxor_G19_Result12 (N58)

MUXF5:I0->O 1 0.314 0.681 Combinationallogic/Mxor_G19_Result1_f5 (PO_OBUF)

OBUF:I->O 4.909 PO_OBUF (PO)

Total 7.851ns (6.328ns logic, 1.523ns route)

(80.6% logic, 19.4% route)

===

Timing constraint: Default OFFSET OUT AFTER for Clock 'Clk'

Total number of paths / destination ports: 2 / 2

Offset: 7.546ns (Levels of Logic = 2)

Source: XORTree/SF2/Q (FF)

Destination: Sout<1> (PAD)

Source Clock: Clk rising

Data Path: XORTree/SF2/Q to Sout<1>Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

-- ------------

FDC:C->Q 1 0.626 0.851 XORTree/SF2/Q (XORTree/SF2/Q)

LUT2:I1->O 1 0.479 0.681 XORTree/Mxor_XR<1>_Result1 (Sout_1_OBUF)

OBUF:I->O 4.909 Sout_1_OBUF (Sout<1>)

Total 7.546ns (6.014ns logic, 1.532ns route)

(79.7% logic, 20.3% route)

===

Timing constraint: Default path analysis

Total number of paths / destination ports: 8 / 3

```
Delay:          9.515ns (Levels of Logic = 5)
Source:         PI<3> (PAD)
Destination:    PO (PAD)
Data Path: PI<3> to PO
Gate    Net
Cell:in->out    fanout   Delay   Delay  Logical Name (Net Name)
----------------------------------------  ------------
IBUF:I->O        2   0.715   0.915  PI_3_IBUF (PI_3_IBUF)
LUT3:I1->O       6   0.479   1.023  Combinationallogic/G11_or0000_SW0 (N30)
LUT4:I1->O       1   0.479   0.000  Combinationallogic/Mxor_G19_Result12 (N58)
MUXF5:I0->O      1   0.314   0.681  Combinationallogic/Mxor_G19_Result1_f5 (PO_OBUF)
OBUF:I->O            4.909          PO_OBUF (PO)
----------------------------------------
Total              9.515ns (6.896ns logic, 2.619ns route)
(72.5% logic, 27.5% route)
=========================================================================
CPU: 3.54 / 3.68 s | Elapsed : 3.00 / 3.00
Total memory usage is 178640 kilobytes
Number of errors   :    0 (   0 filtered)
Number of warnings:    0 (   0 filtered)
Number of infos    :    2 (   0 filtered)
```

DEVICE UTILIZATION RESULT:

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	8	7,168	1%	
Number of 4 input LUTs	27	7,168	1%	
Logic Distribution				
Number of occupied Slices	16	3,584	1%	
Number of Slices containing only related logic	16	16	100%	
Number of Slices containing unrelated logic	0	16	0%	
Total Number of 4 input LUTs	28	7,168	1%	
Number used as logic	27			
Number used as a route-thru	1			
Number of bonded IOBs	17	141	12%	
IOB Flip Flops	2			
Number of GCLKs	1	8	12%	
Total equivalent gate count for design	257			
Additional JTAG gate count for IOBs	816			

Device Utilization Summary

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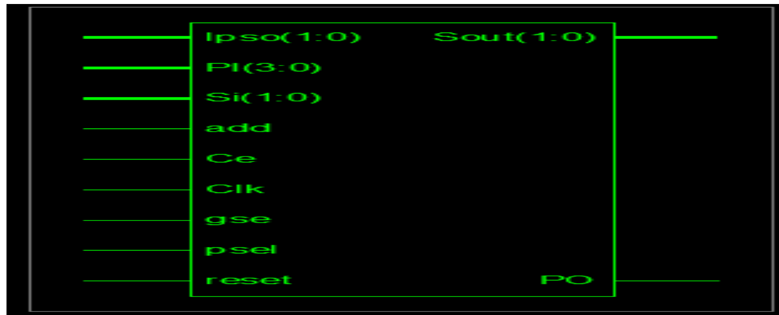
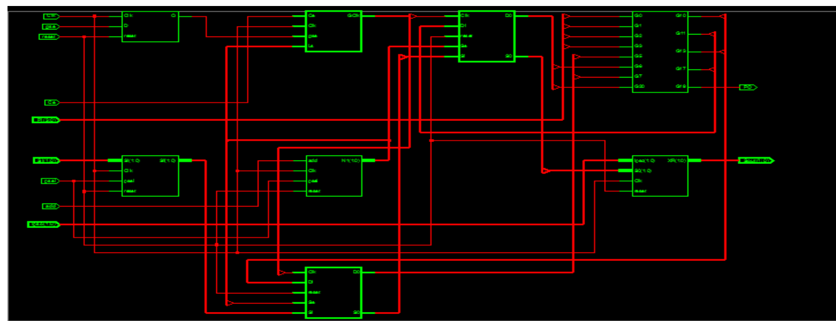
RTL SCHEMATIC

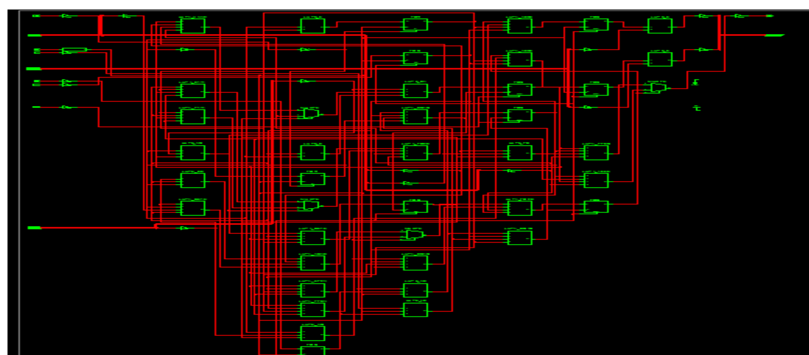


RTL View in Xilinx ISE



Technical Schematic in Xilinx ISE

TECHNOLOGY SCHEMATIC



Technical Schematic of RTL internal view in Xilinx ISE

VSFF:

Netlist File

```
// Generated by Cadence Encounter(R) RTL Compiler v09.10-s233_1
ModuleVSFF (SI, DI, SE, Clk, reset, D0);
Input SI, DI, SE, Clk, reset;
Output D0;
Wire SI, DI, SE, Clk, reset;
Wire D0;
Wire x;
  VDFF SF1 (.D (x), .Clk (Clk), .reset (reset), .Q (D0));
  V2x1Mux SF2 (.in1 (DI), .in2 (SI), .S (SE), .out (x));
end module
```

Area Report

```
============================================================
  Generated by:          Encounter(R) RTL Compiler v09.10-s233_1
  Generated on:          Oct 13 2013 08:18:27 PM
  Module:                VSFF
  Technology library:    tsmc18 1.0
  Operating conditions:  slow (balanced_tree)
  Wireload mode:         enclosed
  Area mode:             timing library
============================================================
Instance  Cells Cell Area  Net Area   Wireload
---------------------------------------------------
VSFF         0        0        0    <none> (D)
(D) = wireload is default in technology library
```

Power Report

```
============================================================
  Generated by:          Encounter(R) RTL Compiler v09.10-s233_1
  Generated on:          Oct 13 2013  08:18:39 PM
  Module:                VSFF
  Technology library:    tsmc18 1.0
  Operating conditions:  slow (balanced_tree)
  Wireload mode:         enclosed
  Area mode:             timing library
```

```
============================================================
              Leakage   Dynamic    Total
Instance Cells Power (nW) Power (nW) Power (nW)
--------------------------------------------
VSFF       0     0.000     0.000     0.000
  SF1      0     0.000     0.000     0.000
  SF2      0     0.000     0.000     0.000
```

Timing Report

```
============================================================
  Generated by:           Encounter(R) RTL Compiler v09.10-s233_1
  Generated on:           Oct 13 2013 08:19:23 PM
  Module:                 VSFF
  Technology library:     tsmc18 1.0
  Operating conditions:   slow (balanced_tree)
Wire load mode:           enclosed
  Area mode:              timing library
============================================================
Pin      Type     Fanout Load Slew Delay Arrival
                  (fF) (ps)  (ps)   (ps)
--------------------------------------------------
SF1/Q   VDFF          1  0.0    0    +0       0 R
D0      out port                     +0       0 R
--------------------------------------------------
Timing slack:  UNCONSTRAINED
Start-point:SF1/Q
End-point    : D0
```

CONCLUSION:

A single cycle access structure is discussed. Various implementations with and without hold mode as well as gated and partial implementation methods are presented. The aspects feasibility, peak power consumption, switching activity during test, area, test cycles, at-speed testing and debugging features are compared. A guide is given how to select the best implementation. The best solution (gSCAS) is compared to RAS implementations and is superior to all known RAS solutions. If BIST is preferable due to limited chip IOs or partial scan implementation, an address controlled BIST is discussed. The ATPG algorithms can be enhanced with the same methods SS implementations are optimized. Future work is related to algorithms for reducing the test cycles per net itself, register reordering, and pattern optimization for activity reduction and de-compression methods for BIST using the gSCAS.

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